91-53530-00A0
Supplement 1
12/6/74

ADDENDUM

MOVING HEAD DISK SYSTEM WITH PERTEC DISK DRIVES

This addendum reflects the changes to the Moving Head Disk System Manual, 91-53530, which describes how to use PERTEC, INC. D3000 series disk drives with Computer Automation Moving Head Disk System.

Paragraph 2.2.6, line 1

Was: ". . . by Diablo disk drives to . . ."

Is: ". . . by Diablo or suitably modified PERTEC disk drives to . . .

Paragraph 2.3.2, line 7 - Insert a new sentence

Was: "or 43 disk drives. For other . . ."

Is: "or 43 disk drives. Figure 2-4 depicts a typical installation for a PERTEC D 3000 series drive. For other . . ."

Paragraph 2.3.2 - Table at end of paragraph, add cable information.

Disk Drive PERTEC D3000 Interface Cable: 81-15264-03

Appendix A, Table A-2 - ADACK signal definition

Was: ". . . from Diablo disk drive only"

Is: ". . . from Diablo or PERTEC disk drives only"

Add Appendix K

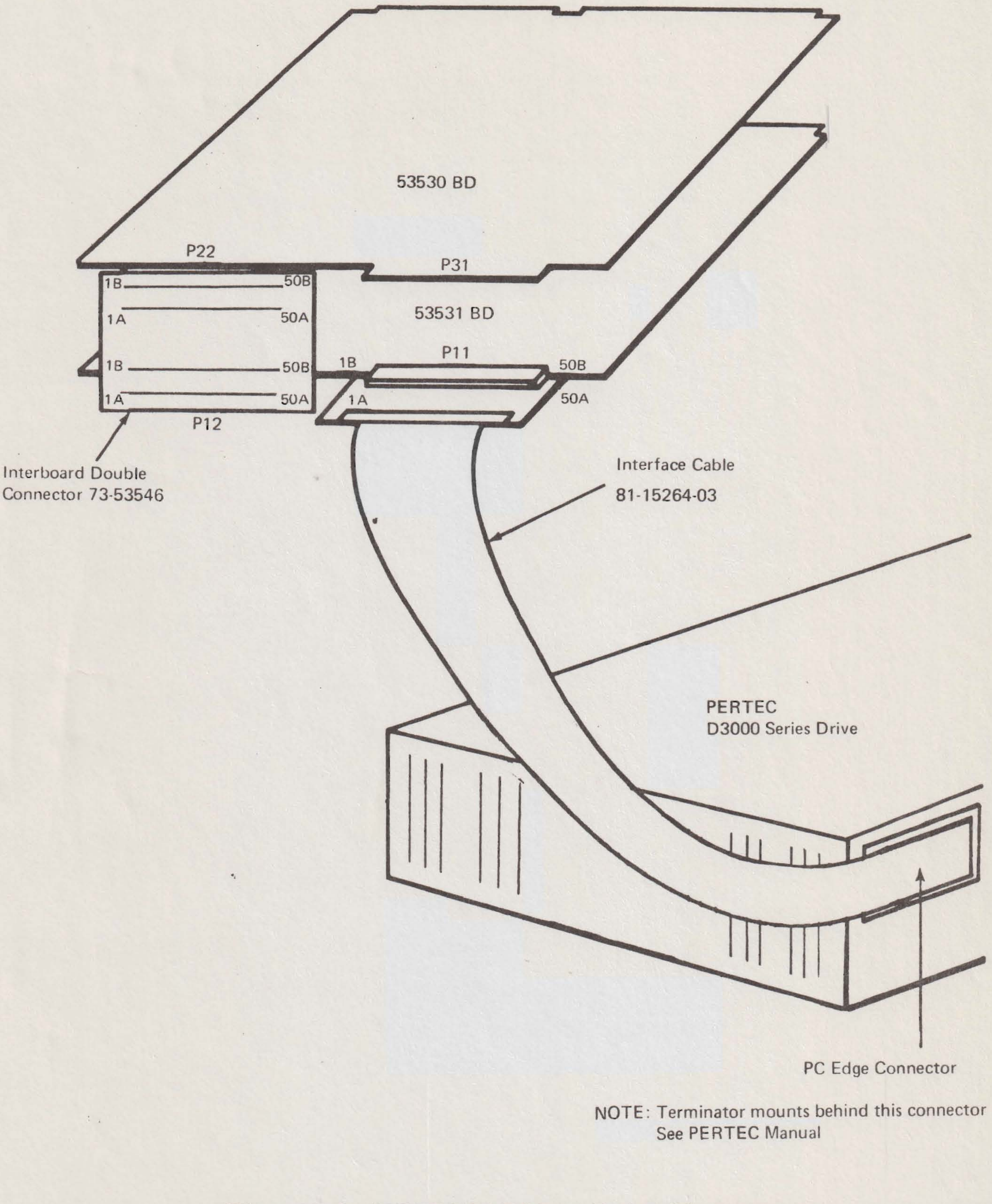
53530 BD
P22
P31
1B
50B
1A
50A
53531 BD
P11
1B
50B
1A
50A
1B
50B
1A
50A
P12
Interboard Double
Connector 73-53546
Interface Cable
81-15264-03
PERTEC
D3000 Series Drive
PC Edge Connector
NOTE: Terminator mounts behind this connector
See PERTEC Manual

Figure 2-4. PERTEC D3000 Installation Diagram

Appendix K

PERTEC DISK DRIVE CONSIDERATIONS

The PERTEC D3000, 100 TPI disk drives used with the Computer Automation Moving Head Disk System must contain PERTEC PC boards configured as shown in Table K-1. Any discrepancy between the tables and the disk drive should be referred to PERTEC, Inc., Chatsworth, California.

The PERTEC disk drives (100 TPI) must be ordered with certain modifications to a basic unit. Table K-2 lists the proper order number for the 100 TPI drives. When ordered under these numbers, the drives should come as detailed in Table K-1. Check the drive against Table K-1 upon arrival to make sure no errors have occurred.

The read/write heads alignment procedure specified in the PERTEC Maintenance Manual (PERTEC Document No. 103715, Paragraph 6.13) must be performed upon arrival to insure interchangeability of disk packs written on different drives (even if both drives are the same model).

NOTE

> PAY SPECIAL ATTENTION TO THE FIRST WARNING NOTE IN PARAGRAPH 6.13.5.2.
>
> Computer Automation uses only Diablo high density, thus steps (1) through (8) inclusive of Paragraph 6.13.5.2 must be performed.

Table K-1. PERTEC PC Board Configurations

PERTEC Board Name	Assembly Number	Check For:
Logic Board	103705-01	Modification installed per PERTEC Modification Drawing 103685 (see back of PERTEC Maintenance Manual for drawing)
or	or	
Logic Board	103685	Components should be installed per Table II, sheet 3 of 3, PERTEC drawing No. 102810, dash number 01 only.
Read/Write Board Diablo Compatible (1500 RPM drives only)	103721-02 (100 TPI) 103721-03 (200 TPI)	Installed in place of assembly 102816. Verify proper components per Table II of 103720 drawing

Table K-1. PERTEC PC Board Configurations (Cont'd)

PERTEC Board Name	Assembly Number	Check For:	
Read/Write Board Diablo Compatible (2400 RPM Drives only)	103721-01 (100 TPI) 103721-03 (200 TPI)	Installed in place of assembly 102816-01. Verify proper components per Table II of 103720 drawing	
Logic Board (For 1500 RPM with mechanical 24 sectors only) 100 TPI or 200 TPI	103705-01 or 103685	Jumper Platform Position	Jumper Assembly Number
		J 121	103611-01
		J 122	103612-01
		J 123	103613-01
		J 124	103614-01
		J 125	103615-01
		J 126	None
		J 127	103616-09
Logic Board (For 2400 RPM with mechanical 24 sectors) 100 TPI or 200 TPI	103705-01 or 103685	J 121	103611-04
		J 122	103612-02
		J 123	103613-02
		J 124	103614-01
		J 125	103615-10
		J 126	None
		J 127	103616-09
Logic Board (For 2400 RPM with electronic 24 sectors) 100 TPI or 200 TPI	103685	J 121	103611-04
		J 122	103612-02
		J 123	103613-02
		J 124	103614-01
		J 125	103615-12
		J 126	103616-09
		J 127	103616-09
Logic Board (For 2400 RPM with electronic 20 sectors) 100 TPI or 200 TPI	103685	J 121	103611-04
		J 122	103612-02
		J 123	103613-02
		J 124	103614-01
		J 125	103615-12
		J 126	103616-08
		J 127	103616-08
Logic Board All units	103685	Verify proper components per Table II of 103684 drawing	

Table K-2. Ordering Information, PERTEC Disk

PERTEC Model No.	PERTEC Order No.	Top Loader or Front Loader	Speed	Tracks Per Inch	Mechanical Number of Sectors
D3321	D3321 -M024 -SSC(SC918)	TOP (5440)	1500 RPM	100	24
D3322	D3322 -M024 -SSC(SC918)	TOP (5440)	2400 RPM	100	24
D3341	D3341- M024- SSC(SC918)	FRONT (2315)	1500 RPM	100	24
D3342	D3342- M024- SSC(SC918)	FRONT (2315)	2400 RPM	100	24

NOTE:
1. Purchase orders should specify "One Shot Read/Write Board Only".
2. For electronic sectoring order -E024 instead of -M024.

COMPUTER AUTOMATION, INC.

the NAKED MINI company

18651 Von Karman, Irvine, Calif. 92664
tel. 714-833-8830 TWX 910-595-1767

MOVING HEAD DISK SYSTEM

91-53530-00A1 August, 1974

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Section 1

GENERAL INFORMATION

1.1 INTRODUCTION

The Computer Automation Moving Head Disk system consists of a controller, cables, and from one to four disk drive units (refer to figure 1-1). The system is designed primarily for Diablo Model 30 and 40 series disk drives, and other drives that are functionally, electrically, and connector compatible to these units. It is intended for use with the NAKED MINI /ALPHA LSI Series computers.

The controller is implemented on two full-sized (15" x 16½") PC boards. Communication between PC boards is provided by a rear-edge interboard connector, while communication with the disk drive(s) is provided by the interface cable which emanates from the rear-edge of one of the two controller boards. The controller consumes approximately 6.5 amps total and operates from 0°C to 50°C.

1.1.1 Applications

Among the myriad applications of the Moving Head Disk system are:

1. Mass data store - data base operation.
2. Mass memory for disk operating systems.
3. Intermediate store for communication store-and-forward message handling.

1.1.2 Features

The primary features of the Moving Head Disk system are as follows:

1. DMA operation which minimizes program control of the interface.
2. Pre-recorded sector formats include error checking for enhanced reliability.
3. One controller can handle up to four disk drive units.
4. Each unit can have 2, 4, 10 or 20 heads.
5. Each track can have any even number of sectors up to 32 (12 standard).
6. Each sector can contain from 16 to 256 data words in increments of 16 (256 standard).

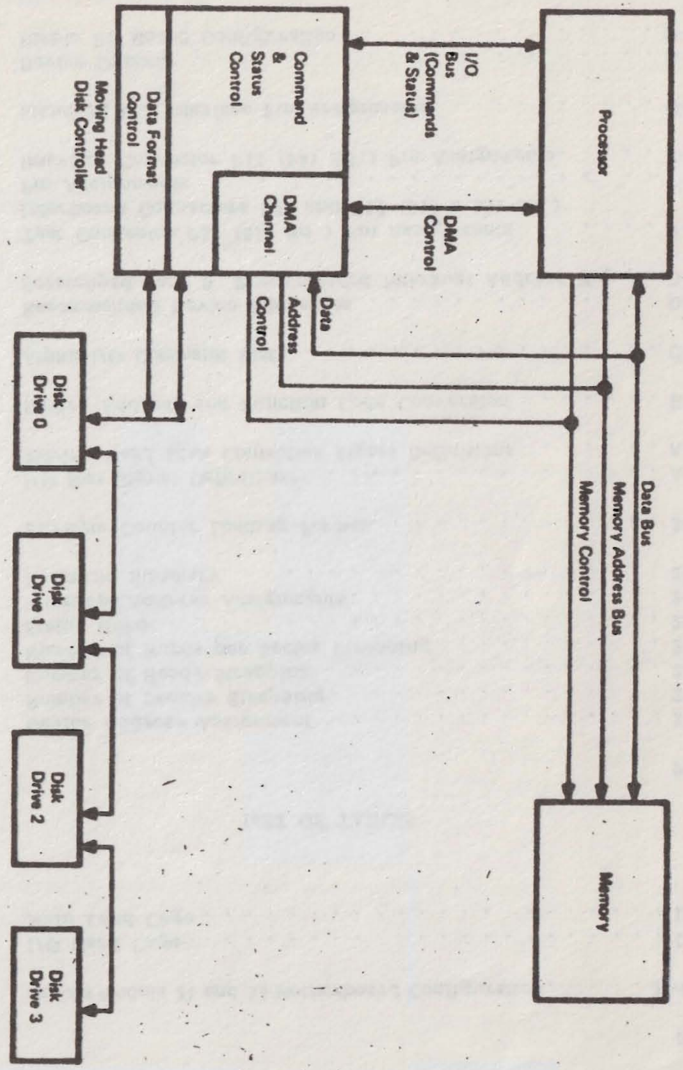

Processor
I/O Bus (Commands & Status)
Command & Status Control
DMA Control
DMA Channel Control
Data Format Control
Moving Head Disk Controller
Data
Address
Control
Data Bus
Memory Address Bus
Memory Control
Memory
Disk Drive 0
Disk Drive 1
Disk Drive 2
Disk Drive 3

Figure 1-1. Moving Head Disk System, Simplified Block Diagram

7. Multiple sector, or partial sector transfers.

8. Sectors are processed consecutively.

9. Bit transfer rates of 1.562 MHz (one 16-bit word each 10.24 μs) or 2.5 MHz (one 16-bit word each 6.4 μs.).

10. Multiple head operations (more than one track of data transferred in one operation).

11. Simultaneous seek operations in all "on-line" disk drives.

12. Operation under interrupts.

13. Flag bits are available for designating alternate track, defective track, system track, user track, etc.

1.2 DISK CONFIGURATION

Each disk platter is divided into cylinders, heads, and sectors (refer to figure 1-2).

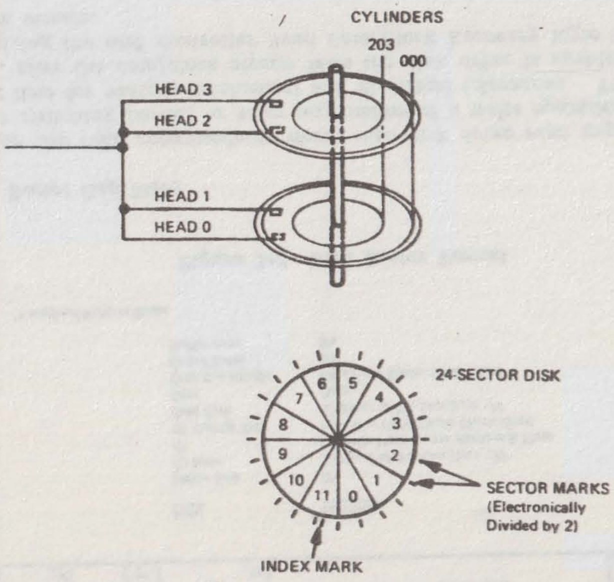


Figure 1-2. Disk Platter Configuration Diagram

Cylinders run around the periphery of each platter, starting at Cylinder 0 (outermost) and going inward to the highest numbered cylinder which depends upon the type of disk drive used (203 or 204, or 406 or 408). Cylinders carry through vertically into all platters of a particular disk drive. Cylinder addresses relate to both sides of all platters. Tracks are sometimes mentioned in relation to cylinders. Tracks are the same as the cylinders, except they relate only to one side or the other of a particular platter.

Heads are associated with each side of a platter. There are two heads per platter, starting at Head 0 (bottommost) and running upward to the topmost, which can be Head 1 (1 platter), Head 3 (2 platters), or up to Head 19 if a disk drive configuration containing 20 heads is used. (Note that on some disk drives the head numbering may be in the opposite direction i.e. Head 0 topmost.) All heads on a given drive move in unison when a "seek" operation is in progress, and all are located at the same cylinder upon completion of the seek operation.

Sectors are pie-shaped divisions of the disk platter. The sectors are numbered from 0 through the maximum numbered sector which is normally 11. Twelve sectors are standard with the system, but the controller can accommodate 8, 10, 12, 20 or 24 sectors. Twenty-four sector disk platters are normally used, with the sectors being electronically divided by two to form 12 effective sectors. The first full sector after detection of the Index mark is considered Sector 0. The Index mark is located just after the start of the maximum numbered mechanical sector.

1.3 RECORDING METHOD

Data is recorded in blocks of up to 256 words per sector in the Data field of a sector. The number of words per sector varies inversely with the number of sectors, i.e., the more sectors, the smaller the data block. (Standard for the system is 12 sectors at 256 words per sector.) Each sector is pre-formatted by recording the cylinder, head, and sector address along with the associated cyclic check word, various flag bits, and guard byte fields which correspond to each sector. (Refer to Sector Format, paragraph 1.3.1.) After the disk is formatted, subsequent operations access the specified cylinder-head-sector and verify correct positioning before performing the specified function.

1.3.1 Sector Format

The following is a description of each field in a sector. (Refer to figure 1-3.)

Sector Gap	ID Sync	ID	ID Cyc Ck Wd	Data Sync	Data	DATA Cyc Ck Wd	Guard Bytes	Buffer Area
24*	16* :7F	4*	2*	32* :7F	512 Max* (256 Words)	2*	8*	≈51*

Field	Contents
Sector Gap	0's
ID Sync	15 Bytes of 0's, Last Byte :7F
ID	Cylinder-Head-Sector Address & Flags
ID Cyc Ck Wd	Identifier Field Cyclic Check Word
Data Sync	31 Bytes of 0's, Last Byte :7F
Data	Data
Data Cyc Ck Wd	Data Field Cyclic Check Word
Guard Bytes	0's
Buffer Area	0's

*Length of Field in Bytes

Figure 1-3. Disk Sector Format

1.3.1.1 Sector Gap Field

The Sector Gap field accommodates worst-case disk drive read amplifier recovery time after switching heads, or after termination of a write operation. It also allows sufficient time for various mechanical and electrical tolerances. The last portion of the field, after the data/clock stream from the disk drive is enabled, is used for synchronizing the disk controller Read Data/Clock Recovery logic to the incoming data/clock stream.

1.3.1.2 Identifier Sync Field

The Identifier (ID) Sync field is used to search for the Sync character in the incoming data which is contained in the last byte of the field.

1.3.1.3 Identifier Field

The ID field contains the cylinder-head-sector address of that sector. On any given track, the ID fields of all sectors will be identical except for the sector number.

1.3.1.4 Identifier Cyclic Check Word Field

The Identifier Cyclic Check Word field contains the cyclic check word for the ID field. This is an even-parity summary of the "1" bits for each bit position (0-15) in the ID field. It is used for error checking.

1.3.1.5 Data Sync Field

The last half of the Data Sync field stabilizes the Read Data - Read Clock separat circuit for reading the Data field. (See ID Sync description, paragraph 1.3.1.2.) The first half allows for worst-case read-to-write switching times during Write Data operations. (ID field is read and compared, after which writing commences if the specified sector was found.) Zeros are written in the field, except for the last byte which is written as :7F to identify the beginning of the Data field.

1.3.1.6 Data Field

The Data field contains the stored data written in 16-bit words.

1.3.1.7 Data Cyclic Check Word Field

The Data Cyclic Check Word field contains the cyclic check word associated with the Data field. (See Identifier Cyclic Check Word field description, paragraph 1.3.1.4.)

1.3.1.8 Guard Bytes Field

The Guard Bytes field is written immediately after the Data Cyclic Check Word field is written. This is to move the head far enough away from the Data Cyclic Check Word field to ensure that no noise spike will occur in that field when the write amplifier is turned off.

1.3.1.9 Buffer Area

The Buffer Area between sectors allows time for write-to-read switching, read amplifier recovery, and disk speed variations.

1.4 FUNCTIONAL DESCRIPTION

Any of the various read or write functions possible on the Moving Head Disk syst (except Write Format) start at the designated cylinder-head-sector on the selected disk drive, and continue until the Direct Memory Access (DMA) word count equal zero, or the end-of-cylinder is reached. (Write Format starts at the designated cylinder-head, but at Sector 0 only.) The operation is first performed on the specified sector, and then higher numbered sectors for the same cylinder-head address until the maximum numbered sector is processed (11 on 12-sector disk).

Heads are then switched (present head disabled and next higher numbered head enabled) and the operation commences at Sector 0 of the next higher numbered head (same cylinder). The 12 sectors associated with the new head are processed, after which heads are again switched (if this was not the last available head). The operation continues in this manner up the cylinder until the word count equals zero, or until the last sector for the last head is processed. The word count not being equal to zero when the last sector has been processed constitutes an error condition.

The general sequence of events to initiate a particular function is listed in chronological order below:

1. The operating program issues an Output command which transfers a 16-bit memory address to the disk controller. The memory address specifies the starting location of the four word Disk Control block which contains the necessary information to perform the required function.
2. The controller initiates four DMA cycles to extract the four control words from Memory.
3. A seek operation is initiated on the selected disk drive to the specified cylinder.
4. The appropriate head is enabled and the specified sector is found.
5. The specified function is performed using the DMA channel.
6. An interrupt is initiated upon completion (if interrupts are enabled).

1.4.1 Disk Control Block

A brief description of each of the four words contained in the Disk Control block is given below. A detailed description of each word is provided in Section 2.

1. Word 1. Contains the starting head and sector addresses, as well as flag bits which may be used to designate alternate cylinder, defective cylinder, write protect, etc.
2. Word 2. Contains the cylinder address, the command (function to be performed), and specified disk drive number. The word also contains two flag bits which can be used for the same purposes as those in Word 1.
3. Word 3. Contains the count of the number of data words to be transferred. The designated function normally ends upon completion of the sector in which the word count has been decremented to zero.

4. Word 4. Contains the starting DMA address which designates the starting location of the data field in Memory.

1.4.2 Disk Functions

Each function performed by the Moving Head Disk system is briefly described in the following paragraphs.

1.4.2.1 Write Data

The Write Data function writes data on the selected disk drive, starting at the specified cylinder-head-sector and continuing until the specified number of words have been transferred or the end-of-cylinder is reached.

1.4.2.2 Read Data

The Read Data function reads data from the selected disk drive, starting at the specified cylinder-head-sector and continuing until the specified number of words has been transferred or the end-of-cylinder is reached.

1.4.2.3 Read Data (Hog Mode)

The Read Data (Hog Mode) function operates the same as the Read Data function, except Memory becomes totally committed to the disk controller. The Processor will not be able to access Memory until termination of the command. The hog mode is normally used only by the Autoload option.

1.4.2.4. Read Identifier

The Read Identifier function transfers the contents of the ID and ID Cyclic Check Word fields of the first sector encountered at the specified cylinder-head, to three successive locations in a designated block of Memory. If the DMA word count is not decremented to zero after the 3-word transfer, the contents of subsequent ID and ID Cyclic Check Word fields will also be transferred to Memory, until the word count equals zero.

1.4.2.5 Read Verify

The Read Verify function checks for errors by comparing the cyclic check words of the ID and Data fields to the recalculated cyclic check words after reading these fields. The operation starts at the specified cylinder-head-sector in the selected

disk drive and ends when the specified number of sectors, as designated by the word count, has been checked or the end-of-cylinder is reached.

1.4.2.6 Seek Cylinder Only

The Seek Cylinder Only function moves the heads in the selected disk drive to the specified cylinder. Overlapping (simultaneous) seek only operations can be done on more than one disk drive.

1.4.2.7 Write Format

The Write Format function "formats" each sector by writing the cylinder-head-sector address and associated cyclic check word, and also the gap, sync, and guard bytes fields which correspond to each sector. Formatting begins at the specified cylinder-head and Sector 0 only, and continues until the specified number of sectors has been formatted or the end-of-cylinder is reached.

1.4.2.8 Miscellaneous Operations

Miscellaneous operations performed with the controller or selected disk drive include:

1. **NO-OP which can be used to "select" a disk drive. (Used prior to reading status or doing a Restore operation.)**
2. **Sense input which interrogates the status of certain functions associated with the controller or disk drive(s).**
3. **Status, residual word count, or Data cylic check word input to Processor. The status word contains the status of various functions associated with the controller or disk drive.**
4. **Restore which "restores" the heads in the selected disk drive to Cylinder 0.**
5. **Enable interrupts.**

Section 2

INTERFACE AND PROGRAMMING CONSIDERATIONS

2.1 GENERAL

This section provides detailed interconnection data for interfacing with the disk drive(s), procedures for assignment of device and interrupt addresses, and programming considerations for the Moving Head Disk system. General programming information may be found in the NAKED MINI/ALPHA LSI Series Programming Reference manual (document number 10077-00).

2.2 BASIC WIRING CONSIDERATIONS

All wiring necessary to implement the Moving Head Disk controller and associated disk drive(s) as a system is included in the prewired interface signal cable and interboard connector which accompany the system when shipped. A portion of this wiring may vary depending upon the system in which it is implemented. This wiring falls into the following categories:

1. Device address assignment.
2. Sector mark divide-by-two implementation.
3. Number of sectors assignment.
4. Number of heads assignment.
5. Number of words per sector assignment.
6. Address acknowledge implementation.
7. Seek complete polarity correction.
8. Interrupt address assignment.

If a change to any of these wiring categories is required, refer to the information provided in paragraphs 2.2.1 through 2.2.7, or 2.17.4 in the case of interrupt address assignment. If no changes are required, proceed to paragraph 2.3 which describes the installation of the interboard connector and interface cable.

2.2.1 Device Address Assignment

The "standard" device address of the Moving Head Disk controller is :0F (hex). This address is preassigned at the factory by jumpering appropriate Peripheral Select pins to ground on rear-edge connector J11. Assignment of this particular address was made to avoid possible future conflict by expanding to other I/O modules, and also because disk diagnostics employ this address. However, if it is necessary to change the device address to one of the other 30 which are possible, it is first necessary to remove any

Table 2-1. Device Address Assignment

PS4- (A5)	PS3- (A4)	PS2- (A3)	PS1- (A2)	PS0- (A1)	DEVICE ADDRESS (Hex)
					0(1)
				X	1
			X		2
			X	X	3
		X			4
		X		X	5
		X	X		6
		X	X	X	7
	X				8
	X			X	9
	X		X		A
	X		X	X	B
	X	X			C
	X	X		X	D
	X	X	X		E
	X	X	X	X	F(2)
X					10
X				X	11
X			X		12
X			X	X	13
X		X			14
X		X		X	15
X		X	X		16
X		X	X	X	17
X	X				18
X	X			X	19
X	X		X		1A
X	X		X	X	1B
X	X	X			1C
X	X	X		X	1D
X	X	X	X		1E
X	X	X	X	X	1F

1. Do not use. Reserved for Processor mounted options and certain control instructions.

2. Standard device address.

3. Associated pin numbers on connector J11 of 531 board are given below signal mnemonic.

jumpers which do not apply to the desired address, and then to connect a jumper (to ground) for the PS4- signal, if required. Table 2-1 indicates with X's the appropriate jumpers for all 31 possible device addresses. Pins B2 and B3 of J11 on the 531 board are at ground potential.

CAUTION

> Device address :00 should not be used. This address is reserved for Processor mounted options and certain control instructions. Using it will cause improper operation of the Processor. Furthermore, a device interface connector containing properly installed device address jumpers must be applied to the rear-edge connector (531 J11) at all times. If it is not, a default address of :00 will be assigned to the module, causing the same problem referred to above.

2.2.2 Sector Mark Divide-By-Two Implementation

Sector mark divide strapping provides electronic division of the received Sector marks by a factor of two. For example, if a disk pack provides 24 Sector marks, and the platter(s) is divided into 12 effective sectors, the sector mark divide strapping must be implemented. To do this, connect a jumper between the following two pins on interface connector J11 of the 531 board.

MNEMONIC	PIN NO.	MNEMONIC	PIN NO.
2SECCL	J11-A16	SECTX	J11-A17

2.2.3 Number of Sectors Assignment

The number of effective sectors contained on each platter must be assigned for detection of last sector (the maximum numbered sector). This is done by strapping the appropriate pins on interface connector J11 of the 531 board to ground as denoted by X's in table 2-2. Ground potential is provided at pins J11-B2 and B3.

Table 2-2. Number of Sectors Strapping

NO. OF SECTORS	SECTOR NUMBERS	SS04- (A27)	SS03- (A26)	SS02- (A25)	SS01- (A24)	SS00- (A23)
8	0-7		X	X	X	X
10	0-9		X			X
12	0-11		X		X	X
20	0-19	X			X	X
24	0-23	X		X	X	X

Notes:

1. Strapping for a number of sectors other than those shown is possible, but not recommended.
2. Twelve is considered the "standard" number of effective sectors
3. Pin numbers (in parenthesis) associated with connector J11 on 531 board.

2.2:4 Number of Heads Assignment

The number of heads used with the disk drive(s) in the system must be assigne for detection of end-of-cylinder. This is done by strapping the appropriate pins on interface connector J11 of the 531 board to ground if 4, 10, or 20 heads are used, and leaving all three pins open if only two heads are used. Strapping information is provided in the chart below. Ground is at pins J11-B2 and B3.

Table 2-3. Number of Heads Strapping

NO. OF HEADS	HEAD NUMBERS	MNEMONIC	STRAP TO GND
2	0-1		N/C
4	0-3	4STRAP-	J11-A22
10	0-9	10STRAP-	J11-A18
20	0-19	20STRAP-	J11-A21

2.2.5 Number of Words per Sector Assignment

The number of data words associated with each sector must be assigned for control purposes. This is done by installation of a jumper between the JMP-outp pin and the appropriate input pin (JMP2- thru JMP5-) on interface connector J11 of the 531 board. The standard number of 256 words (512 bytes), which is used with 12 or 10 sectors, does not require strapping. See "JMP" in Table A- for complete strapping.

Table 2-4. Number of Words per Sector Strapping

WORDS/ SECTOR	BYTES/ SECTOR	STRAP JMP-(J11-A28) TO: MNEMONIC	PIN NO.
256	512		N/C
240	480	JMP2-	J11-A30
224	448	JMP3-	J11-A31
192	384	JMP4-	J11-A32
128	256	JMP5-	J11-A33

2.2.6 Address Acknowledge

The address acknowledge signal (ADACK) is generated by Diablo disk drives to indicate acceptance of the cylinder address. The signal is input at pin B8 on interface connector J11 of the 531 board. For all other types of disk drives, this signal pin must be strapped to ground. Ground potential is provided at pins J11-B2 and B3.

2.2.7 Seek Complete Polarity Correction

The seek complete (SCOM0-SCOM3) signal(s) from on-line disk drive(s) may or may not be of the correct polarity for integration with controller logic. The signals are passed through a polarity correction network to ensure correct polarity. The network is controlled by the static input signal SCPOL which is at pin B5 on interface connector J11 of the 531 board. If the SCOM input signals are negative-true ("1" = 0 Vdc) SCPOL should be grounded. If the SCOM signals are positive-true ("1" = +5 Vdc), SCPOL should be left open. Ground is available at pins B2 and B3 of connector J11.

2.3 INSTALLATION

2.3.1 PC Board

The Moving Head Disk controller consists of two full-sized PC boards (part nos. 53530 and 53531). The boards are inserted into the motherboard together with the 53530 on top. Note that placement of the two disk controller PC boards within a processor or expansion chassis is critical due to DMA priority and Memory Banking chains, and also the unidirectional communications capability of DMA modules with memory. For proper placement of these boards, refer to section 2 of the Computer Handbook - 91-20400-00.

2.3.2 Interboard and Interface Cabling (figures 2-1, 2-2, and 2-3)

Signal connections between the 530 and 531 boards are made via the interboard PC board connector (part no. 73-53546) which is shown in figures 2-1, 2-2 and 2-3. Installation of the connector is as shown in the drawings (pins B50 and A50 to the right when facing from the rear). The interface cable is also installed as shown with pins B50 and A50 to the right.

Figures 2-1, 2-2 and 2-3 depict typical installations when using the Diablo Model 31, 33, or 43 disk drives. For other types of disk drives, the interboard and interface cabling is the same. Cabling at the disk drive(s) will vary however. Refer to the manuals included with the disk drive for this information, or contact Computer Automation, Inc.

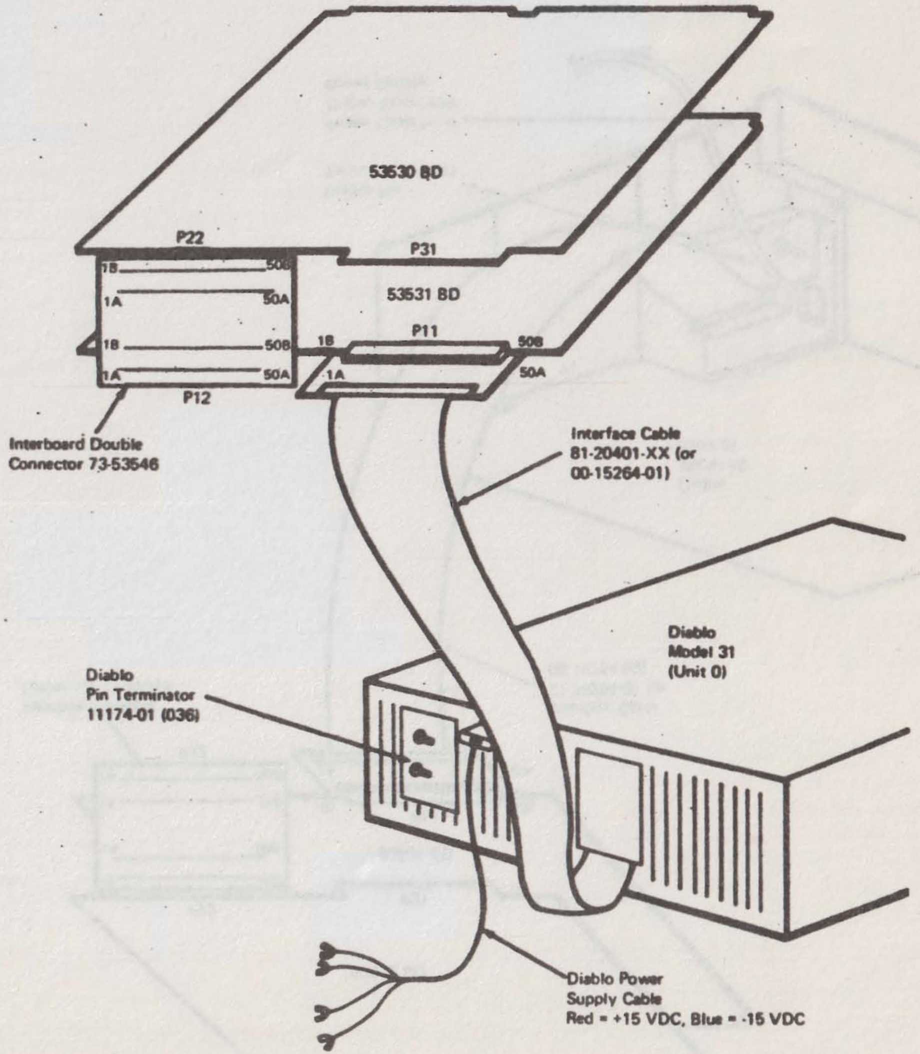

53530 BD
P22
P31
1B
50B
1A
50A
53531 BD
P11
1B
50B
1A
50A
1B
50B
1A
50A
P12
Interboard Double Connector 73-53546
Interface Cable 81-20401-XX (or 00-15264-01)
Diablo Model 31 (Unit 0)
Diablo Pin Terminator 11174-01 (036)
Diablo Power Supply Cable
Red = +15 VDC, Blue = -15 VDC

Figure 2-1. Diablo Model 31 Installation Diagram

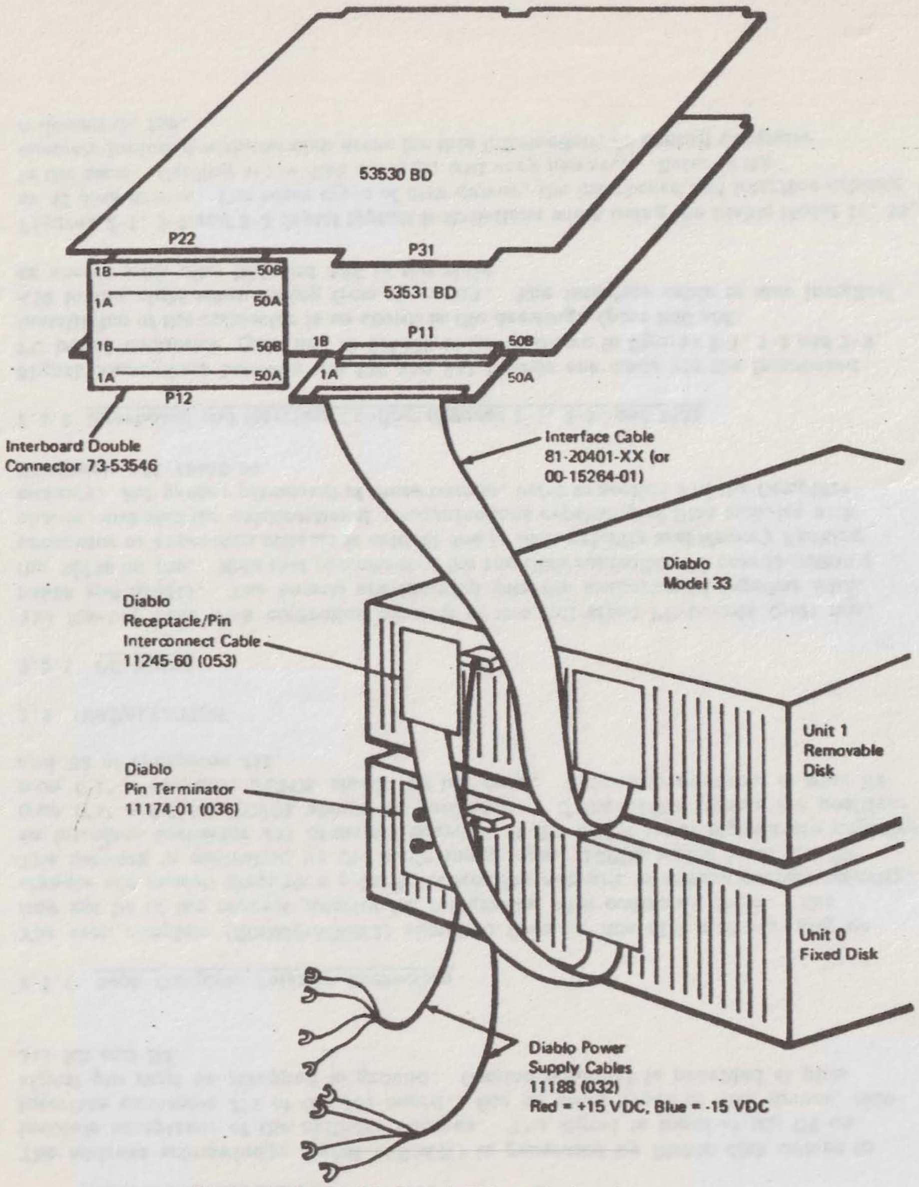

53530 BD
P22
P31
1B
50B
1A
50A
53531 BD
P11
1B
50B
1A
50A
1B
50B
1A
50A
P12
Interboard Double Connector 73-53546
Interface Cable 81-20401-XX (or 00-15264-01)
Diablo Model 33
Diablo Receptacle/Pin Interconnect Cable 11245-60 (053)
Unit 1 Removable Disk
Diablo Pin Terminator 11174-01 (036)
Unit 0 Fixed Disk
Diablo Power Supply Cables 11188 (032) Red = +15 VDC, Blue = -15 VDC

Figure 2-2. Diablo Model 33 Installation Diagram

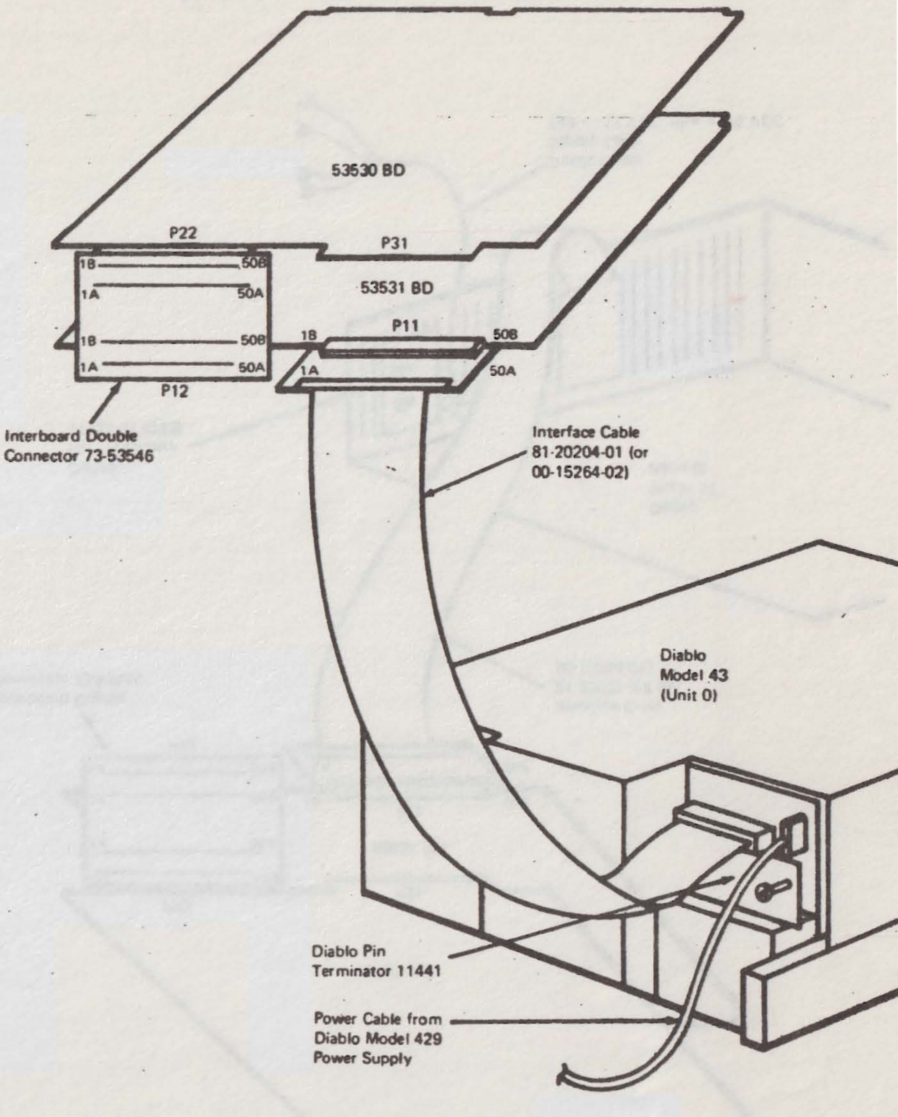

53530 BD
P22
P31
1B
50B
1A
50A
53531 BD
P11
1B
50B
1A
50A
1B
50B
1A
50A
P12
Interboard Double Connector 73-53546
Interface Cable 81-20204-01 (or 00-15264-02)
Diablo Model 43 (Unit 0)
Diablo Pin Terminator 11441
Power Cable from Diablo Model 429 Power Supply

Figure 2-3. Diablo Model 43 Installation Diagram

Interface cables required for the Moving Head Disk systems are as follows:

DISK DRIVE	INTERFACE CABLE
Diable Mod 31 and 33	81-20401-XX
Diablo Mod 43	81-20204-01
All others	Contact Computer Automation, Inc.

2.4 INITIALIZATION

Initialization places the Moving Head Disk controller into a known static state. The disk controller is initialized by issuing a Select command with a device address of :F and a function code of 3. It is also initialized when the system reset (RST) is activated by depressing the RESET switch on the control panel, or when the hardware powerup sequence is taking place in the Processor. Initialization of the disk controller has the following characteristics:

1. Disable interrupts
2. Clear any pending interrupts
3. Clear all error flags
    a. Rate error
    b. Head address error
    c. Identifier cyclic check word error
    d. End-of-cylinder error
    e. No identifier compare
    f. Timeout period exceeded
4. Clear Seek Complete status flags and other circuitry pertaining to seek complete. (Does not disable any Seek operation in progress.)
5. Clear circuitry pertaining to Restore operations. (Does not disable any Restore operation(s) already in progress at the disk drive(s).)
6. Select Unit O
7. Institute idle condition for disk controller.

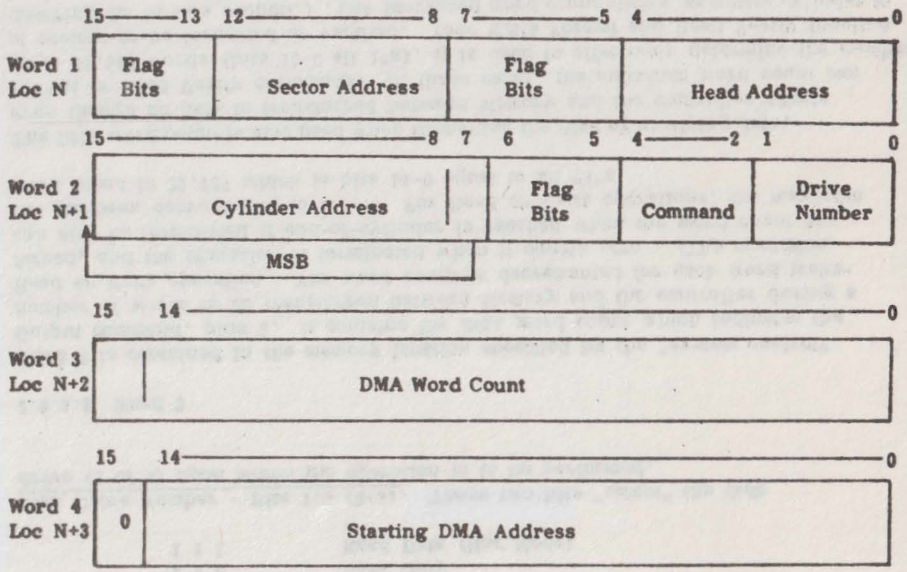
2.4.1 Initialization Coding

```
(label) SEL    F,3
```

2.5 SYSTEM CONTROL

2.5.1 Four-Word Disk Control Block

The Moving Head Disk system is controlled by outputting a four-word Disk Control block to the controller. The control block is contained in four sequential memory locations whose addresses are arbitrary. Transfer of the control block to the controller is initiated by an Output command which transfers the beginning address of the control block (contained in the A or X register) to the controller, and initiates four DMA cycles to extract the information from Memory. The information includes the disk drive number, command, cylinder address, head address, sector address, DMA word count, and the starting DMA address. A control block must be output to the controller for each operation performed. A format of each word is shown below, and a description of each is provided in the following paragraphs.



2.5.1.1 Word 1

Word 1 is contained in the memory location specified by the "system control" Output command. A description of each portion of the word follows:

Flag Bits - Bits 15-13. These bits are forced to zero during Write Format. Then during any data transfer operation these bits must be set by the program to all zero's otherwise a No ID Compare error will occur. It is not enough just to have the correct cylinder, head, and sector addresses. The flag bits are also compared to the identifier written in each sector.

Sector Address - Bits 12-8 (12 = MBS). Contains the starting sector address (any one, 0 through maximum numbered sector). The sector address is automatically incremented as each sector is processed (for multiple sector operations), and set to 0 as the maximum numbered sector is processed (for multiple head operations). The maximum numbered sector is determined by Number of Sectors Assignment - paragraph 2.2.3.

Flag Bits - Bits 7-5. Same as bits 15-13.

Head Address - Bits 4-0 (4 = MSB). Contains the starting head address (any one, 0 through maximum numbered head). The head address is automatically incremented after the maximum numbered sector is processed (for multiple head operations). The maximum numbered head is determined by Number of Heads Assignment - paragraph 2.2.4.

2.5.1.2 Word 2

Word 2 is contained in the memory location specified by the "system control" Output command, plus 1. A description of each portion of the word follows:

Cylinder Address - Bits 15-7 (8 = LSB, 7 = MSB). Contains the address of the cylinder to be used in the operation. The cylinder address is not incremented since multiple cylinder operations are not possible. If a 203 or 204 cylinder disk drive is used, the cylinder address is contained in bits 15-8, with bit 8 as the LSB. If a 406 or 408 cylinder disk drive is used, bit 7 becomes the MSB for addresses 256 through 405 or 407.

Flag Bits - Bits 6,5. Same as bits 15-13 of Word 1.

Command - Bits 4-2. These bits designate the operation to be performed. The bit formats and associated commands are given in the chart below:

4 3 2	COMMAND
0 0 0	NO-OP
0 0 1	Read Data
0 1 0	Read Identifier
0 1 1	Read Verify
1 0 0	Write Data
1 0 1	Write Format
1 1 0	Seek Only
1 1 1	Read Data (Hog Mode)

Disk Drive Number - Bits 1,0 (0-3). These two bits "select" the disk drive (1 of 4) upon which the operation is to be performed.

2.5.1.3 Word 3

Word 3 is contained in the memory location specified by the "system control" Output command, plus 2. It contains the DMA word count which indicates the number of words to be transferred between Memory and the controller during a Read or Write operation. The word count is decremented for each word transferred, and the operation is terminated when it equals zero. (The operation can also be terminated if end-of-cylinder is reached when the word count has not yet been decremented to zero.) For Read or Write operations, the maximum word count is 32,767 which is bits 14-0 equal to all "1"s.

The DMA word count is also used when formatting the disk or verifying data, even though no data is transferred between Memory and the controller (Write Format or Read Verify command). In these cases, the maximum word count can go to 65,535 words (bits 15-0 all 1"s). It is used to effectively determine the nu of sectors to be formatted or verified. (See Write Format and Read Verify functi descriptions in this section.) The increased word count allows an entire cylinder be formatted or verified, even in the maximum configuration where 20 heads are used.

2.5.1.4 Word 4

Word 4 is contained in the memory location specified by the "system control" Out command, plus 3. It contains the starting DMA address in Memory where the fir data word will be extracted during a Write operation, or stored during a Read operation. The DMA address is incremented (within the disk controller) for eac word transferred, so data words are extracted from, or stored in progressively higher numbered memory locations. The highest numbered location possible is 32,767 (bits 14-0 equal to all "1's).

2.5.2 Programming Considerations

The four word Disk Control block is transferred to the controller via the DMA channel as controlled by the disk controller. The DMA sequence to extract the four words from Memory is initiated by an Output command with a device address of :F ("standard" address for disk controller) and a function code of 0. The Output command also transfers the starting address (in Memory) of the Disk Control block to the controller, which should have been previously loaded into the A (or X) register. Refer to the NAKED MINI/ALPHA LSI Series Programming Reference manual for the types of Output commands possible. Both conditional and unconditional Output commands may be used. The command format follows:

```
(label)        INST    F,0
```

where:

INST = one of the NAKED MINI/ALPHA LSI Output commands

2.6 SENSE FUNCTION

Sense commands determine the status of functions relating to the controller, selected disk drive, or in the case of "seek complete", to all on-line disk drives. Each function is interrogated by issuing a Sense command with a device address of :F, and a function code which relates only to the interrogated function. (See Programming considerations below.) If the function is true, a true response is sent to the Processor. If the function is false, no response is sent.

2.6.1 Programming Considerations

There are two Sense commands used by the NAKED MINI/ALPHA LSI computer. Refer to the NAKED MINI/ALPHA LSI Series Programming Reference manual for a full description of each. The Sense command format follows:

```
(label)        INST    F,FC
```

where:

INST = one of the NAKED MINI/ALPHA LSI Sense commands
FC = function code, which determines function interrogated, according to the following:

FC	DESCRIPTION
0	Controller not busy
1	Controller not busy
2	1. Selected disk drive not ready, or 2. Selected disk drive unsafe (write check) or 3. Timeout period exceeded
3	Seek error at selected disk drive
4	Seek complete at Disk Drive 0
5	Seek complete at Disk Drive 1
6	Seek complete at Disk Drive 2
7	Seek complete at Disk Drive 3

2.7 STATUS, WORD COUNT, OR DATA CYCLIC CHECK WORD INPUT

The status of the controller and selected disk drive is input to the Processor by issuing an Input command with a device address of :F and a function code of 0. The remaining DMA word count, or the Data cyclic check word can be input in the same manner by simply using a different function code. (See Programming Considerations below.) The information is placed in the Processor A or X register, depending upon the command used.

There are 16 status indications associated with the status word. These are listed in table 2-5. They are input to the A or X register in the same bit order. Certain of the status indications are stored in the controller by turning on associated flags. These flags are turned off upon execution of an Input command using a function code of 0 (status input). These flags are noted with an X in the FLAGS RESET column. Each status condition is described in detail in appendix A under its associated mnemonic.

2.7.1 Programming Considerations

A number of Input commands may be used to input the status, word count, or Data cyclic check word, both unconditional and conditional. Refer to the NAKED MINI/ALPHA LSI Series Programming Reference manual for descriptions of the various types of Input commands. If a conditional Input command is used, the function code will cause interrogation of the same functions referred to under SENSE FUNCTION, Programming Considerations, paragraph 2.5.1. The Input command format follows:

```
(label)   INST    F,FC
```

where:

INST = one of the NAKED MINI/ALPHA LSI Input commands
FC = function code which determines the type of information to be input (and the function sensed for conditional inputs) as follows:

FC	DESCRIPTION
0	Input status
1	Input word count
2	Input Data cyclic check word

NOTE

To ensure proper status conditions in the controller relative to the disk drive, a Status input should be done upon completion of all operations (including Restore) except NO-OP and Initialize.

2.8 WRITE DATA FUNCTION

The Write Data function causes data to be written on the selected disk drive, starting at the specified cylinder-head-sector, and continuing until the DMA word count equals zero. Data is extracted from Memory by DMA cycles, starting at the location specified by the DMA address, and subsequently from consecutively higher locations. The Data cyclic check word is written in each sector, following the Data field. If the end-of-cylinder is reached with the WC ≠ 0, or an error condition exists at the selected disk drive, early termination will occur.

2.8.1 Programming Considerations

Implementation of the Write function requires the considerations listed below in chronological order.

Table 2-5. Status Word

BIT	FLAGS RESET	MNEMONIC	DESCRIPTION (WHEN BIT = 1)
0		CBUSY	Controller busy
1	X	IDCOME	No identifier compare
2	X	IDCCE	Identifier cyclic check word error
3	X	DACCE	Data cyclic check word error
4	X	EOC	End-of-cylinder (with WC ≠ 0)
5	X	HAERF	Head address error
6	X	RATER	DMA rate error
7	X	TIMEOUT	Timeout period exceeded
8		DRDY-	Selected disk drive not ready
9		UNSAFE	Selected disk drive "unsafe" (write check)
10		SEEKER	Seek error
11	X	SCD0-	Seek not complete, disk drive 0
12	X	SCD1-	Seek not complete, disk drive 1
13	X	SCD2-	Seek not complete, disk drive 2
14	X	SCD3-	Seek not complete, disk drive 3
15		WRPTCT	Selected disk drive write protected

2.8.1.1 Sense Function - Paragraph 2.6

The Sense function determines the status of the disk controller. The controller must be "not busy" before proceeding. (The Sense function is not required if a conditional Output command is used for the System Control function which follows.)

2.8.1.2 System Control - Paragraph 2.5

System control sets up the following conditions with the controller and disk drive(s):

1. Disk drive selection
2. Cylinder selection
3. Head selection
4. Sector selection
5. Write Data command
6. Flag bits (if necessary)
7. DMA word count
8. DMA starting address

2.8.1.3 Sense Function - Paragraph 2.6

The Sense function can be used during the Write Data operation to determine time of completion (controller not busy).

2.8.1.4 Status Input - Paragraph 2.7

Status input is used upon completion of the Write Data operation to determine if any error conditions have occurred.

2.8.2 Interrupts

As an alternative to the Sense function, it may be desirable to initiate a Processor interrupt upon completion of the Write Data operation (when the word count (WC) equals zero), or when the operation is terminated by an error condition (end-of-cylinder reached and WC ≠ 0, etc.). This is accomplished by enabling interrupts at the disk controller by issuing an Output command with the appropriate device address and a function code of 3. Interrupts are further explained in paragraph 2.17.

2.9 READ DATA FUNCTION

The Read Data function causes data to be read from the selected disk drive, starting at the specified cylinder-head-sector, and continuing until the word count equals zero. Data words received from the disk are transferred to the memory location specified by the DMA address. The DMA address is incremented by one after each transfer, and the DMA word count is decremented by one. If the end-of-cylinder is reached with the WC ≠ 0, or an error condition exists at the selected disk drive, early termination will occur.

2.9.1 Programming Considerations

Implementation of the Read Data function requires the considerations listed below in chronological order.

2.9.1.1 Sense Function - Paragraph 2.6

The Sense function determines the status of the disk controller. The controller must be "not busy" before proceeding. (The Sense function is not required if a conditional Output command is used for the System Control function which follows.)

2.9.1.2 System Control - Paragraph 2.5

System control sets up the following conditions with the controller and disk drive(s):

1. Disk drive selection
2. Cylinder selection
3. Head selection
4. Sector selection
5. Read Data command
6. Flag bits (if necessary)
7. DMA word count
8. DMA starting address

2.9.1.3 Sense Function - Paragraph 2.6

The Sense function can be used during the Read Data operation to determine time of completion (controller not busy).

2.9.1.4 Status Input - Paragraph 2.7

Status input is used upon completion of the Read Data operation to determine if any error conditions have occurred.

2.9.2 Interrupts

As an alternative to the Sense function, it may be desirable to initiate a Processor interrupt upon completion of the Read Data operation (when WC = 0) or when the operation is terminated by an error condition (end-of-cylinder reached and WC ≠ 0, etc.). This is accomplished by enabling interrupts at the disk controller by issuing an Output command with the appropriate device address and a function code of 3. Further insight into the use of interrupts with the disk controller is provided in paragraph 2.17.

2.10 READ DATA (HOG MODE) FUNCTION

The Read Data (Hog Mode) function (sometimes referred to as "burst mode") operates in exactly the same manner as the Read Data function except Memory becomes totally committed to the disk controller. The Processor will not be able to access Memory until termination of the command. This occurs when the DMA word count is decremented to zero, or the end-of-cylinder is reached. The hog mode is normally reserved for the Processor Autoload option only.

2.10.1 Programming Considerations

Implementation of the Read Data (Hog Mode) function, requires the considerations listed below in chronological order.

2.10.1.1 Sense Function - Paragraph 2.6

The Sense function determines the status of the disk controller. The controller must be "not busy" before proceeding. (The Sense function is not required if a conditional Output command is used for the System Control function which follows.)

2.10.1.2 System Control - Paragraph 2.5

System control sets up the following conditions with the controller and disk drive(s):

1. Disk Drive selection
2. Cylinder selection
3. Head selection

4. Sector selection
5. Read Data (Hog Mode) command
6. Flag bits (if necessary)
7. DMA word count
8. DMA starting address

2.10.1.3 Sense Function - Paragraph 2.6

The Sense function can be used during the Read Data (Hog Mode) operation to determi time of completion (controller not busy).

2.10.1.4 Status Input - Paragraph 2.7

Status input is used upon completion of the Read Data (Hog Mode) operation to determine if any error conditions have occurred.

2.10.2 Interrupts

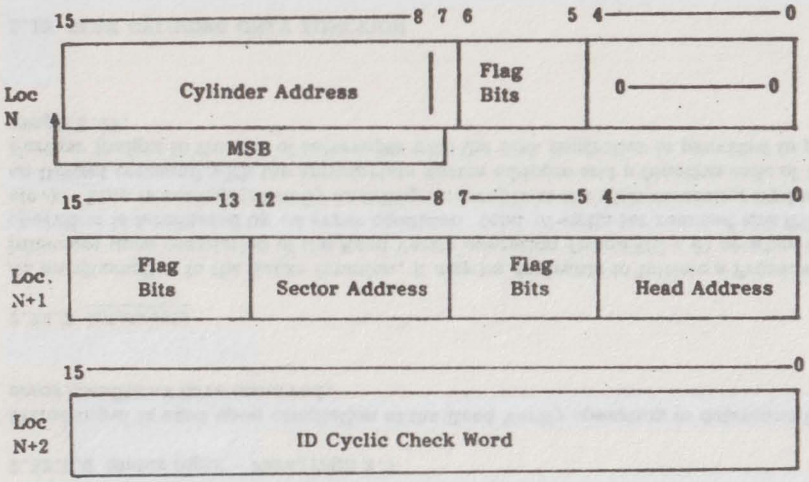
As an alternative to the Sense function, it may be desirable to initiate a Processor interrupt upon completion of the Read Data (Hog Mode) operation (when WC = 0) or when the operation is terminated by an error condition (end-of-cylinder reached and WC ≠ 0, etc.). This is accomplished by enabling interrupts at the disk controlle by issuing an Output command with the appropriate device address and a function cod of 3. Further insight into the use of interrupts with the disk controller is provided in paragraph 2.17.

2.11 READ IDENTIFIER FUNCTION

The Read Identifier function first seeks the designated cylinder and enables the designated head. It then transfers the contents of the Identifier field of the first sector encountered to Memory, placing the information in three consecutive locations starting at the designated DMA address. The DMA word count must be equal to at least three for all the information to be transferred.

The contents of the Identifier field of subsequent sectors may also be transferred to Memory by simply increasing the DMA word count by three for each additional Identifier field desired. The additional information will be placed in successive 3-word blocks until the word count is decremented to zero. If the end-of-cylinder is reached with the WC ≠ 0, or an error condition exists at the selected disk drive, early termination will occur.

The contents of the memory locations will be as follows:



2.11.1 Programming Considerations

Implementation of the Read Identifier function requires the considerations listed below in chronological order.

2.11.1.1 Sense Function - Paragraph 2.6

The Sense function determines the status of the disk controller. The controller must be "not busy" before proceeding. (The Sense function is not required if a conditional Output command is used for the System Control function which follows.)

2.11.1.2 System Control - Paragraph 2.5

System control sets up the following conditions with the controller and disk drive(s):

1. Disk Drive selection
2. Cylinder selection
3. Head selection

4. Read Identifier command
5. Flag bits (if necessary)
6. DMA word count (3X no. of sector ID fields to be read)
7. DMA starting address

2.11.1.3 Sense Function - Paragraph 2.6

The Sense function can be used during the Read Identifier operation to determine time of completion (controller not busy).

2.11.1.4 Status Input - Paragraph 2.7

Status input is used upon completion of the Read Identifier operation to determine if any error conditions have occurred.

2.11.2 Interrupts

As an alternative to the Sense function, it may be desirable to initiate a Processor interrupt upon completion of the Read Identifier operation (when WC = 0) or when the operation is terminated by an error condition. This is accomplished by enabling interrupts at the disk controller by issuing an Output command with the appropriate device address and a function code of 3. Further insight into the use of interrupts with the disk controller is provided in paragraph 2.17.

2.12 READ VERIFY FUNCTION

The Read Verify function compares the cyclic check word of the Identifier and Data fields to the recalculated cyclic check word after reading these fields. If either does not compare, an associated flag is turned on. The state of both flags may be interrogated by inputting status. The comparing begins at the designated cylinder-head-sector, and ends when the DMA word count is decremented to zero. The DMA word count is decremented by one for each "data" word received. (The data is not transferred to Memory.) The maximum word count can be 65,535 which is more than sufficient to allow an entire cylinder to be verified, even if the maximum configuration of 20 heads is used. If the end-of-cylinder is reached with the WC ≠ 0, or an error condition exists at the selected disk drive, the operation will terminate.

2.12.1 Programming Considerations

Implementation of the Read Verify function requires the considerations listed below in chronological order.

2.12.1.1 Sense Function - Paragraph 2.6

The Sense function is used to determine the status of the disk controller. The controller must be " not busy" before proceeding. (The Sense function is not required if a conditional Output command is used for the System Control function which follows.)

2.12.1.2 System Control - Paragraph 2.5

System control sets up the following conditions with the controller and disk drive (s):

1. Disk drive selection
2. Cylinder selection
3. Head selection
4. Sector selection
5. Read Verify command
6. Flag bits (if necessary)
7. DMA word count (no. of sectors to be verified X no. of words per sector)

2.12.1.3 Sense Function - Paragraph 2.6

The Sense function can be used during the Read Verify operation to determine time of completion (controller not busy).

2.12.1.4 Status Input - Paragraph 2.7

Status input is used upon completion of the Read Verify operation to determine if any error conditions have occurred.

2.12.2 Interrupts

As an alternative to the Sense function, it may be desirable to initiate a Processor interrupt upon completion of the Read Verify operation (when WC = 0) or when the operation is terminated by an error condition (end-of-cylinder reached and WC ≠ 0, etc.). This is accomplished by enabling interrupts at the disk controller by issuing an Output command with the appropriate device address and a function code of 3. Further insight in the use of interrupts with the disk controller is provided in paragraph 2.17.

2.13 SEEK CYLINDER ONLY FUNCTION

The Seek Cylinder Only function causes the heads in the selected disk drive to move to the specified cylinder. The controller's portion of the operation normally terminates prior to the heads reaching the specified cylinder ("seek complete"). This is to allow seek operations to occur on more than one disk drive, essentially at the same time. The head-sector address, as well as the DMA word count and starting address are transferred to the controller, but are of no consequence since they are unused.

2.13.1 Programming Considerations

Implementation of the Seek Cylinder Only function requires the considerations listed below in chronological order.

2.13.1.1 Sense Function - Paragraph 2.6

The Sense function determines the status of the disk controller. The controller must be "not busy" before proceeding. (The Sense function is not required if a conditional Output command is used for the System Control function which follows.)

2.13.1.2 System Control - Paragraph 2.5

System control sets up the following conditions with the controller and disk drives:

1. Disk drive selection
2. Cylinder selection
3. Seek Cylinder Only command

2.13.1.3 Sense Function - Paragraph 2.6

The Sense function can be used during the Seek Cylinder Only operation to determine when the controller's portion of the seek operation is completed (controller not busy). This does not necessarily mean the heads are over the addressed cylinder (seek complete).

The Sense function can be used after the controller goes "not busy" to determine the following:

1. Seek complete at disk drive 0, 1, 2 or 3
2. Seek error at selected disk drive.

2.13.1.4 Status Input - Paragraph 2.7

Status input is used upon completion of the controller's portion of the Seek Cylinder Only operation to determine if any error conditions have occurred. It can also be used to determine seek complete at disk drives 0, 1, 2 or 3.

2.13.2 Interrupts

As an alternative to the Sense function, it may be desirable to initiate a Processor interrupt upon completion of the Seek Cylinder Only operation. This can be done by enabling interrupts at the disk controller by issuing an Output command with the appropriate device address and a function code of 3. Further insight into the use of interrupts with the disk controller is provided in paragraph 2.17.

2.14 WRITE FORMAT FUNCTION

The Write Format function "formats" each sector by recording the cylinder-head-sector address and associated cyclic check word, and also the necessary gap, sync, and guard bytes fields which correspond to each sector. The Data field is filled with zeros. The formatting begins at the specified cylinder-head address and Sector 0 only, and continues until the DMA word count equals zero. The DMA word count is decremented by one for each word of zeros written. As an example, if 12 sectors associated with a particular cylinder-head address are to be formatted, and each sector is capable of storing 256 words, then a DMA word count of 3072 is required to format all 12 sectors. The maximum word count can be 65,535 which is more than sufficient to allow an entire cylinder to be formatted in one operation, even if the maximum configuration of 20 heads is used. No actual data is transferred from Memory and the DMA starting address included with the four-word Disk Control block is of no consequence. If the end-of-cylinder is reached with the WC ≠ 0, or an error condition exists at the selected disk drive, the operation will terminate.

2.14.1 Programming Considerations

Implementation of the Write Format function requires the considerations listed below in chronological order.

2.14.1.1 Sense Function - Paragraph 2.6

The Sense function determines the status of the disk controller. The controller must be "not busy" before proceeding. (The Sense function is not required if a conditional Output command is used for the System Control function which follows.)

2.14.1.2 System Control - Paragraph 2.5

System control sets up the following conditions with the controller and disk drive(s):

1. **Disk drive selection**
2. **Cylinder selection**
3. **Head selection**
4. **Sector selection (0 only)**
5. **Write Format command**
6. **Flag bits (to indicate alternate cylinder, write protect, etc.)**
7. **DMA word count (no. of sectors to be formatted X no. of words per sector)**

2.14.1.3 Sense Function - Paragraph 2.6

The Sense function can be used during the Write Format operation to determine time of completion (controller not busy).

2.14.1.4 Status Input - Paragraph 2.7

Status input is used upon completion of the Write Format operation to determine if any error conditions have occurred.

2.14.2 Interrupts

As an alternative to the Sense function, it may be desirable to initiate a Processor interrupt upon completion of the Write format operation (when WC = 0) or when the operation is terminated by an error condition (end-of-cylinder reached and WC ≠ 0, etc.). This is accomplished by enabling interrupts at the disk controller by issuing an Output command with the appropriate device address and a function code of 3. Further insight into the use of interrupts with the disk controller is provided in paragraph 2.17.

2.15 NO-OP COMMAND

The NO-OP command is used to "select" the specified disk drive, possibly in conjunction with the Restore command or Status input function. No other action is taken by the controller or selected disk drive, except to update the cylinder-head-sector address, the DMA starting address, and the DMA word count with whatever is contained in the Disk Control block transferred from Memory. This is of no consequence however, since this information is updated with all functions performed (except Restore).

The NO-OP command does not place the controller in a "busy" status. The busy status is unnecessary because the operation terminates after the fourth word of the Disk Control block is transferred from Memory, and since the words are transferred in the DMA "burst" mode, no Processor instructions can be executed during the transfer.

2.15.1 Programming Considerations

Implementation of the NO-OP command requires the considerations listed below in chronological order.

2.15.1.1 Sense Function - Paragraph 2.6

The Sense function determines the status of the disk controller. The controller must be "not busy" before proceeding. (The Sense function is not required if a conditional Output command is used for the System Control function which follows.)

2.15.1.2 System Control - Paragraph 2.5

System control sets up the following conditions with the controller and disk drive (s):

1. Disk drive selection
2. NO-OP command

2.15.1.3 Sense Function - Paragraph 2.6

The Sense function can be used upon completion of the NO-OP function to determine if the selected disk drive is ready. It is not used, as is the case in other operations, to determine when the controller goes "not busy" since the controller never does go busy during a NO-OP.

2.15.1.4 Status Input - Paragraph 2.7

Status input is used upon completion of the NO-OP to determine the status of the controller and selected disk drive.

2.15.2 Interrupts

Interrupts are not used with the NO-OP command.

2.16 RESTORE COMMAND

The Restore command causes the heads on the selected disk drive to be "restored" to Cylinder 0. It is normally used when a seek error condition exists at the selected drive. The seek error condition will remain true until the restore operation is initiated.

2.16.1 Programming Considerations

To implement the Restore operation upon occurrence of a seek error, it is first necessary to determine the presence of a seek error from the selected disk drive. This is normally done by implementing the Status input function upon completion or early termination of the operation being performed. The Sense function can also be used to determine the presence of a seek error.

Status Input - paragraph 2.7
Sense Function - paragraph 2.6

Upon determination that a seek error does exist at the selected disk drive, the Restore operation is initiated by issuing a Select command with a device address of :F ("standard" address) and a function code of 4. The command format follows:

```
(label)      SEL     F,4
```

Completion of the Restore operation is signalled by the disk drive via its seek complete (SCOM0, 1, 2 or 3) line. These lines can be monitored by Status input or the Sense function. (Refer to paragraph 2.7 or 2.6 respectively.)

NOTE

> Ensure that any previous Seek operation is complete before attempting a Restore operation. When the Restore operation is complete, a Status input must be done.

2.16.2 Interrupts

As an alternative to Status input or the Sense function, it may be desirable to initiate a Processor interrupt upon completion of the Restore operation. This can be done by enabling interrupts at the disk controller by issuing an Output command with a device address of :F and a function code of 3. Further insight into the use of interrupts with the disk controller is provided in paragraph 2.17.

2.17 PROCESSOR INTERRUPTS

Processor interrupts are used when the Processor must respond to an event in the shortest possible time, or when it is undesirable for the Processor to wait in a "sense" loop for a particular event to occur. The events which may generate an interrupt from the disk controller fall into two categories:

1. Process Halt (includes end-of-operation)
2. Seek Complete

Each of the categories is explained below under Interrupt Descriptions.

One interrupt channel is provided by the disk controller, along with an associated software controlled enable. The interrupt is enabled by issuing an Output command with the appropriate device address and a function code of 3. It is disabled when an interrupt request is serviced by the Processor. All events which are capable of initiating an interrupt activate the one interrupt channel. It is then necessary to implement the Status Input function (paragraph 2.7) to determine the cause of the interrupt.

When interrupts have been enabled, and the interrupt channel is activated by a Process Halt or Seek Complete event occurring (see Interrupt Descriptions, paragraph 2.17.1), and no other interrupts are presently being processed by the Processor, then an interrupt request is generated if no higher priority device has also requested an interrupt. The Processor's response will be an interrupt address request.

The interrupt address supplied by the disk controller in response to the address request vectors the Processor to a memory location containing the interrupt instruction associated with the disk controller. (Refer to Interrupt Address Assignment, paragraph 2.17.4). Besides enabling the interrupt address to be transferred to the Processor, the interrupt address request disables further interrupts from the disk controller until they are once again enabled by another Output command having a function code of 3.

2.17.1 Interrupt Descriptions

2.17.1.1 Process Halt Interrupt

A Process Halt interrupt can occur upon completion of various operations initiated by the System Control function (end-of-operation), or when disk operations terminate early due to an error condition. The events which can initiate a Process Halt interrupt are listed below:

1. End-of-Operation
   - a. Write Data (WC = 0 and end-of-sector)
   - b. Read Data (WC = 0 and end-of-sector)
   - c. Read Data (Hog Mode) (WC = 0 and end-of-sector)
   - d. Read Verify (WC = 0 and end-of-sector)
   - e. Write Format (WC = 0 and end-of-sector)
   - f. Read Identifier (end-of-sector in which WC goes to 0)
2. Identifier or Data Cyclic Check Word Error. Can occur during any operation other than Write Format, Seek Cylinder Only, and NO-OP, where recalculated Identifier or Data cyclic check word does not compare to the cyclic check words read from the disk.
3. End-of-Cylinder Reached and WC $\neq 0$.
4. Seek Cylinder Only (not an error condition). Occurs upon completion of the controller's portion of a Seek Cylinder Only operation.
5. Unsafe. Occurs when an "unsafe" (write check) condition exists at the selected disk drive.
6. Selected disk drive not ready.
7. Timeout period exceeded.
8. Seek cylinder error at selected disk drive.
9. No ID Compare. No successful Identifier field compare after at least one full revolution of disk at specified cylinder-head address.

Any of these events will turn on the Process Halt flag which subsequently initiates an interrupt, if interrupts are enabled. This flag is turned off when status is input to the Processor.

2.17.1.2 Seek Complete, Disk Drive 0, 1, 2, 3

The Seek Complete interrupt will occur when the seek cylinder operation on any disk drive is complete (heads at specified cylinder) and the controller is not busy. This type of interrupt is normally used in conjunction with Seek Cylinder Only operations, or Restore operations. A seek complete flag is associated with each disk drive. As the seek operation is completed, the associated flag is turned on and an interrupt is initiated if interrupts are enabled (and the controller is not busy). In simultaneous multiple seek operations, if more than one flag is on, only one interrupt will occur. Status input determines that more than one seek operation is complete. Status input also turns off the seek complete flags.

2.17.2 Interrupt Conditions Summary

1. Interrupts must be enabled at the disk controller.
2. The Process Halt, or at least one of the seek complete flags must be on.
3. The Processor must not be servicing interrupts elsewhere in the system.
4. The disk controller must have interrupt priority (no higher priority interrupt request active).
5. The Processor must have interrupts enabled (EIN instruction).

2.17.3 Programming Considerations

Interrupts are enabled at the disk controller by issuing an Output command with the appropriate device address and a function code of 3. They are disabled when an interrupt is serviced by the Processor or the disk controller is initialized (refer to paragraph 2.4). The Output command format follows:

```
        (label)   OTA   F,3
```

Programming considerations are given in chronological order below for the two categories of interrupts.

2.17.3.1 Process Halt Interrupts

1. Enable Interrupts - Paragraph 2.17.3. Interrupts are enabled prior to the System Control function.
2. System Control - Paragraph 2.5.

3. Status Input - Paragraph 2.7. Status input is used after the interrupt occurs to determine its cause. If no error conditions are noted in the status word, the interrupt was caused by the end of an operation. Inputting status will clear the Process Halt flag.

2.17.3.2 Seek Complete Interrupts

1. System Control - Paragraph 2.5. Initiate Seek Cylinder Only operation at specified disk drive.
2. Sense Function - Paragraph 2.6. The Sense function determines when the controller's portion of the seek only operation is completed. If overlapping (simultaneous) seek only operations are to be performed, another System Control function would be done now to initiate seek only in another disk drive.
3. Enable Interrupts - Paragraph 2.17.3. When the seek operation is complete, the associated Seek Complete flag is turned on and the interrupt occurs. If simultaneous seek only operations are taking place, interrupts may have to be re-enabled after the Status Input function below.
4. Status Input - Paragraph 2.7. The Status Input function determines which drive has completed the seek operation. It will also determine of course, if the seek operation was not completed and an error condition occurred (at the selected disk drive only). Inputting status will clear the Seek Complete flag(s) which initiated the interrupt. If simultaneous seek only operations are taking place, and Status Input determines not all have been completed, then interrupts will have to be re-enabled to detect completion of those incomplete operations.

2.17.4 Wiring Considerations

2.17.4.1 Interrupt Address Assignment

The Moving Head Disk controller provides for the generation of a unique interrupt address. The base address for the Processor interrupt is location :000. This address has been displaced to a "standard" address of :00A by strapping on rear-edge connector J11 of the 531 board. This standard address can be changed, if necessary, to other addresses within the first 512 locations of Memory by using interrupt address enable lines E2- through E256-. Grounding a particular enable line pin on rear-edge connector J11 adds the corresponding decimal value to the base location :000. For example, for the "standard" interrupt address of the disk controller, E2- and E8- are grounded to add 10 to the base address, resulting in an address of 10 or :00A (hex).

Table 2-6 lists the interrupt locations available to the disk controller and the corresponding enable line(s) to be grounded to obtain these locations (represented by X's). The straps should be connected to pins B02 or B03 which are at ground potential. Appendix D provides a list of recommended interrupt addresses to prevent possible conflict with other standard I/O modules.

2.18 COMMAND FUNCTION CODE SUMMARY

Table 2-7 is a summary of the eight possible function codes in relation to the various types of commands used with the Moving Head Disk controller.

2.19 NAKED MINI/ALPHA 16 vs. NAKED MINI/ALPHA LSI CONTROLLER

Any disk pack written using the NAKED MINI/ALPHA 16 disk controller will be readable when using the NAKED MINI/ALPHA LSI disk controller.

When using the NAKED MINI/ALPHA 16 disk controller, any Input command executed by the controller, regardless of function code, would cause a status reset and reset any flags previously set. When using the NAKED MINI/ALPHA LSI disk controller, only an Input command using a function code of 0 will cause a status reset (Status input).

2.20 NAKED MINI/ALPHA LSI-1 vs. NAKED MINI/ALPHA LSI-2 USAGE

When using the LSI-1 computer, the disk controller will lock out the CPU from Memory when data transfers begin, and keep it locked out until data transfers cease.

When using the LSI-2 computer, data transfers will occur on a cycle stealing basis and the CPU will not be locked out for more than one memory cycle time.

Table 2-6. Interrupt Address Assignments

E256- (A11)	E128- (A10)	E64- (A09)	E32- (A08)	E16- (A07)	E8- (A06)	E4- (A12)	E2- (A13)	INT ADDR 2 - 3E	INT ADDR 40 - 7E	INT ADDR 80 - BE	INT ADDR C0 - FE
Note 2								0 (5)	40	80	C0
							X	2	42	82	C2
						X		4	44	84	C4
						X	X	6	46	86	C6
					X			8	48	88	C8
					X		X	A (6)	4A	8A	CA
					X	X		C	4C	8C	CC
					X	X	X	E	4E	8E	CE
				X				10	50	90	D0
				X			X	12	52	92	D2
				X		X		14	54	94	D4
				X		X	X	16	56	96	D6
				X	X			18	58	98	D8
				X	X		X	1A	5A	9A	DA
				X	X	X		1C	5C	9C	DC
				X	X	X	X	1E	5E	9E	DE
			X					20	60	A0	E0
			X				X	22	62	A2	E2
			X			X		24	64	A4	E4
			X			X	X	26	66	A6	E6
			X		X			28	68	A8	E8
			X		X		X	2A	6A	AA	EA
			X		X	X		2C	6C	AC	EC
			X		X	X	X	2E	6E	AE	EE
			X	X				30	70	B0	F0
			X	X			X	32	72	B2	F2
			X	X		X		34	74	B4	F4
			X	X		X	X	36	76	B6	F6
			X	X	X			38	78	B8	F8
			X	X	X		X	3A	7A	BA	FA
			X	X	X	X		3C	7C	BC	FC
			X	X	X	X	X	3E	7E	BE	FE
NOTE 1	0	0						2 - 3E			
	0	X							40 - 7E		
	X	0								80 - BE	
	X	X									C0 - FE

NOTES:

1. Additional bits associated with addresses :40 thru :FE.
2. Grounding E256- adds :100 to the interrupt address. For example, locations :002 and :042 would be :102 and :142 respectively.
3. Interrupt locations given in hex.
4. Connector J11 (264 bd.) pin numbers are given below the corresponding enable line, in parenthesis.
5. Location :000 reserved for power fail/restart.
6. Standard interrupt location.

Table 2-7. Command Summary

FUNCTION CODE	SELECT COMMANDS	SENSE COMMANDS	OUTPUT COMMANDS	INPUT COMMANDS
0		Controller not busy	System control	Status input
1		Controller not busy	Same as FC0	DMA word count input
2		1. "Timeout" period exceeded 2. Selected drive: a. Not ready, or b. Unsafe (write check)	Same as FC0	Data cyclic check word input
3	Initialize	Seek error at selected drive	Enable interrupts	
4	Restore selected drive to Cylinder 0	Seek complete at Disk Drive 0	Same as FC0	
5		Seek complete at Disk Drive 1	Same as FC0	
6		Seek complete at Disk Drive 2	Same as FC0	
7		Seek complete at Disk Drive 3	Same as FC0	

Section 3

THEORY OF OPERATION

3.1 GENERAL

This section describes the theory of operation of the Moving Head Disk Controller. The theory is supported by logic diagrams 75-53530 and 75-53531; block diagrams, figure 3-1 through figure 3-7; flow charts, figures 3-8 and 3-16; and various timing diagrams.

3.1.1 Logic Levels

Logic levels, both internal and external to the disk controller, are defined as follows:

INTERNAL (Positive Logic)	TO/FROM CPU (Negative Logic)	TO/FROM DISK DRIVES
1 = +5 VDC	1 = 0 VDC	Mostly negative logic, but some positive. See logic diagrams and disk drive manual(s).
0 = 0 VDC	0 = +5 VDC	

3.2 BLOCK DIAGRAM DESCRIPTION

The relationship between the different functions of the disk controller is given in figure 3-1. Each function is represented by a block. Detailed block diagrams for each function are contained in figures 3-2, 3-3, 3-5, 3-6, and 3-7.

3.2.1 Processor Interface (Figure 3-2)

The Processor Interface provides control of communication between the program and the disk controller. This includes interrupt control, control bus receivers, device code recognition, and sense line control.

3.2.1.1 I/O Data Bus Mux

The I/O Data Bus Mux applies status or DMA word count information to the Data (D) bus lines for transfer to the Processor. Status information is applied to the D bus if an input command with the appropriate device address and a function code 0 is issued. The DMA word count is applied to the D bus if function code 1 is used.

3.2.1.2 Sense Multiplexer

The Sense Multiplexer enables interrogation of ten conditions associated with the controller, selected disk drives, or, in the case of "seek complete", any disk drive. The conditions are interrogated by issuing a Sense command with the appropriate device address and the associated function code. Each function code corresponds to a particular condition or conditions (not ready, "unsafe", rate errors, and "timeout" period exceeded are combined). The ten conditions which may be interrogated are:

Function Code	Functions
0,1	Controller not busy
2	Selected disk drive not ready, "unsafe", rate error or "timeout" period exceeded
3	Seek error at selected disk drive
4	Seek complete at disk drive 0
5	Seek complete at disk drive 1
6	Seek complete at disk drive 2
7	Seek complete at disk drive 3

3.2.1.3 Control Bus Receivers

The Control Bus Receivers buffer the control signal inputs from the Control (C) bus.

3.2.1.4 Device Address Decode

The Device Address decode compares the predetermined device address of the disk controller (Predetermined by jumpers on rear-edge connector J11 of 531 board) with the device address received from the Processor via the P field of the Address (A) bus. A positive comparison enables the disk controller. The "standard" device address assigned to the disk controller is :0F. The address can be changed if necessary. Refer to paragraph 2.2.1.

3.2.1.5 Function Field Receivers

The Function Field Receivers buffer the function code signal inputs (F field of the A bus) received from the Processor.

3.2.1.6 I/O Command Decode

The I/O Command Decode logic decodes various inputs from the C bus and the F field of the A bus to produce certain control signals associated with the execution of Output, Input, or Select commands by the disk controller.

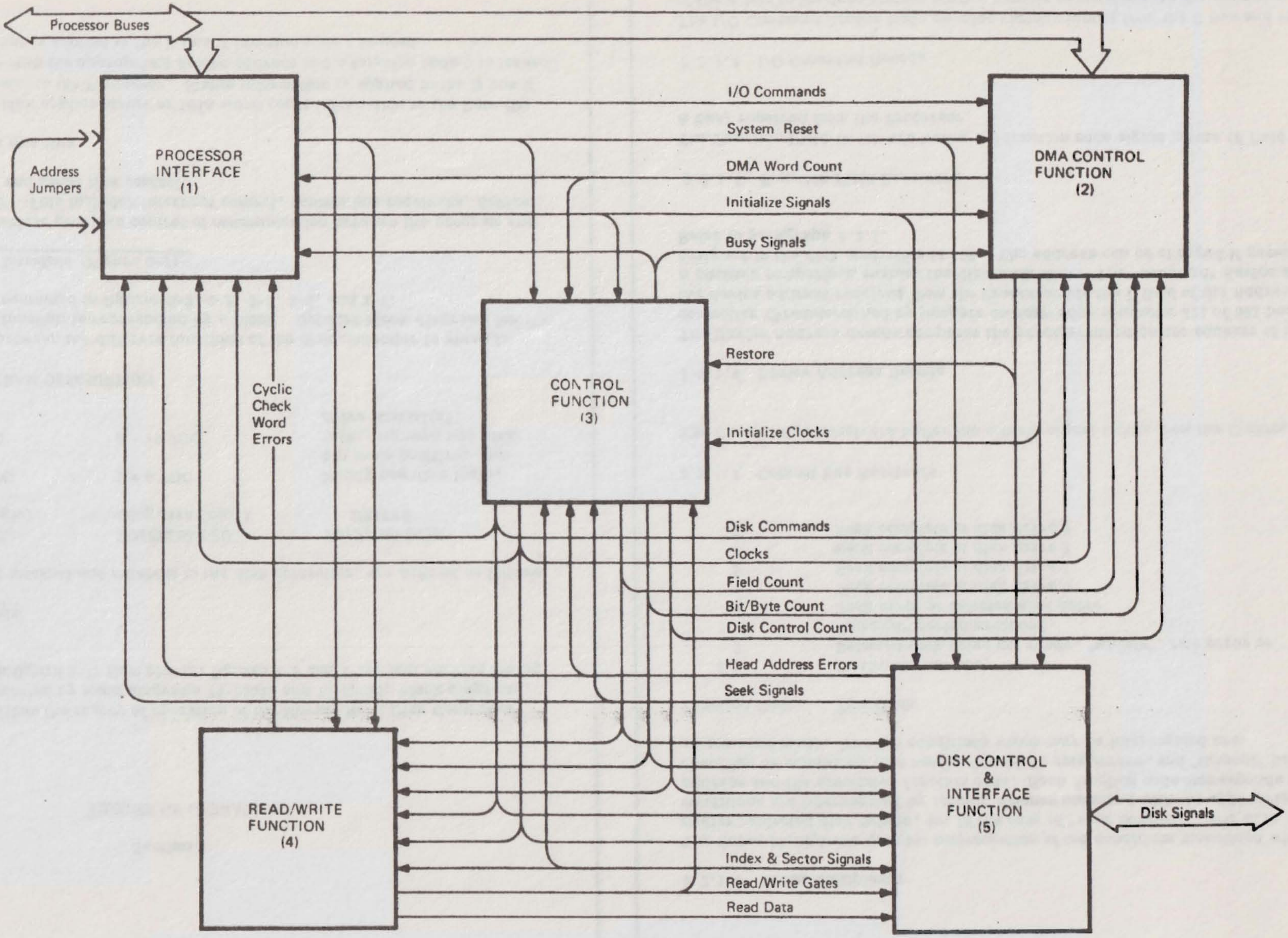
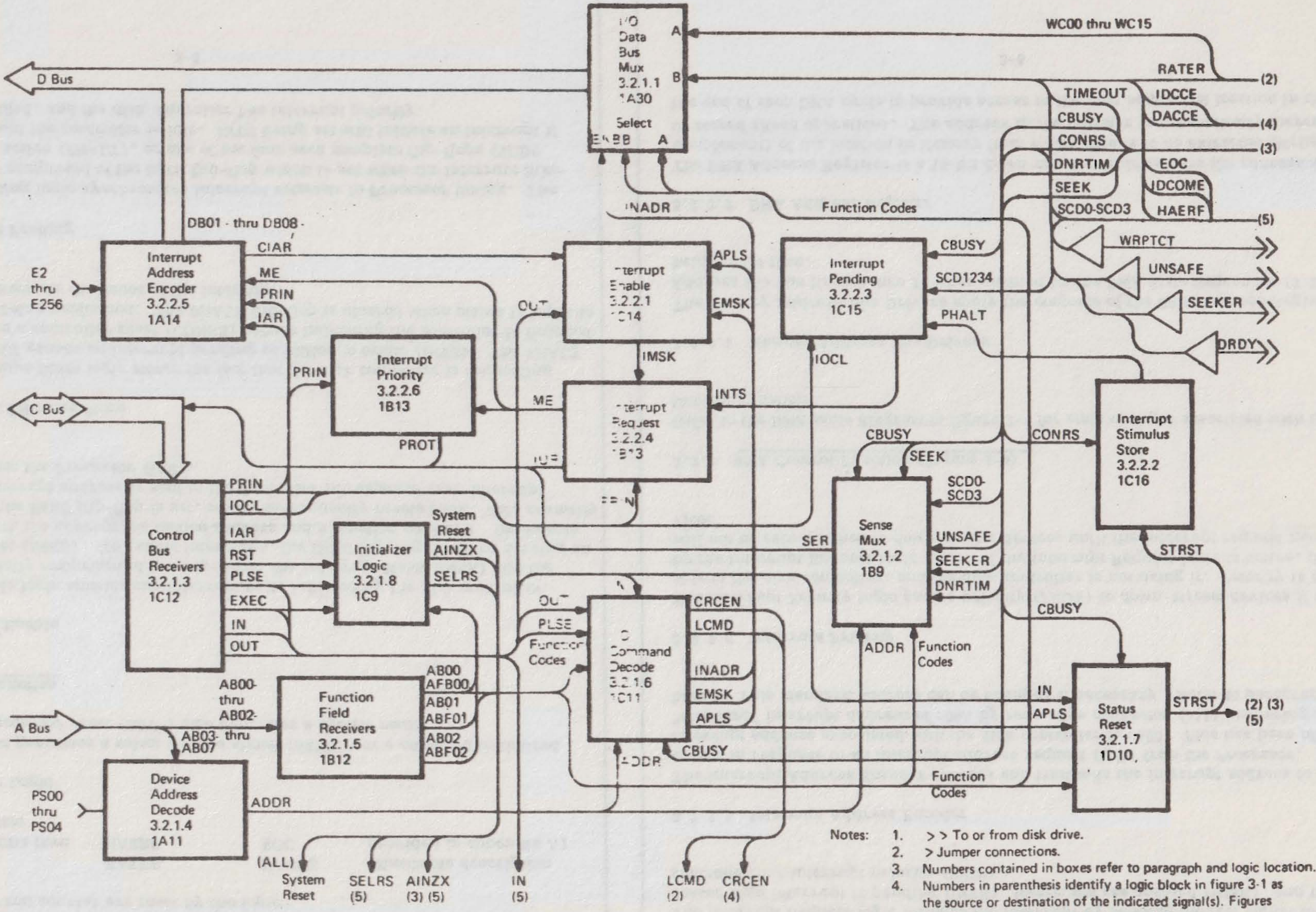

Processor Buses
PROCESSOR INTERFACE (1)
Address Jumpers
DMA CONTROL FUNCTION (2)
I/O Commands
System Reset
DMA Word Count
Initialize Signals
Busy Signals
CONTROL FUNCTION (3)
Restore
Initialize Clocks
Cyclic Check Word Errors
Disk Commands
Clocks
Field Count
Bit/Byte Count
Disk Control Count
Head Address Errors
Seek Signals
READ/WRITE FUNCTION (4)
DISK CONTROL & INTERFACE FUNCTION (5)
Disk Signals
Index & Sector Signals
Read/Write Gates
Read Data

Figure 3-1. Moving Head Disk Controller Block Diagram


I/O Data Bus Mux 3.2.1.1 1A30
A
B
Select
ENBB
A
WC00 thru WC15
RATER
(2)
TIMEOUT
IDCCE
CBUSY
DACCE
(4)
CONRS
(3)
DNRTIM
EOC
SEEK
IDCOME
SCD0-SCD3
HAERF
(5)
WRPTCT
UNSAFE
SEEKER
DRDY
D Bus
DB01 - thru DB08 -
CIAR
Interrupt Address Encoder 3.2.2.5 1A14
E2 thru E256
ME
PRIN
IAR
INADR
Function Codes
Interrupt Enable 3.2.2.1 1C14
APLS
EMSK
OUT
Interrupt Pending 3.2.2.3 1C15
CBUSY
SCD1234
PHALT
IOCL
IMSK
Interrupt Priority 3.2.2.6 1B13
PRIN
ME
PROT
Interrupt Request 3.2.2.4 1B13
INTS
IUF
PRIN
C Bus
Interrupt Stimulus Store 3.2.2.2 1C16
CONRS
CBUSY
SEEK
SCD0-SCD3
Sense Mux 3.2.1.2 1B9
SER
UNSAFE
SEEKER
DNRTIM
STRST
Control Bus Receivers 3.2.1.3 1C12
PRIN
IOCL
IAR
RST
PLSE
EXEC
IN
OUT
System Reset
Initializer Logic 3.2.1.8 1C9
AINZX
SELRS
OUT
PLSE
Function Codes
IN
IO Command Decode 3.2.1.6 1C11
CRCEN
LCMD
INADR
EMSK
APLS
CBUSY
ADDR
ADDR
Function Codes
CBUSY
IN
APLS
Status Reset 3.2.1.7 1D10
STRST
(2) (3) (5)
Function Codes
AB00-thru AB02-
A Bus
AB03- thru AB07
Function Field Receivers 3.2.1.5 1B12
AB00
AFB00
AB01
ABF01
AB02
ABF02
PS00 thru PS04
Device Address Decode 3.2.1.4 1A11
ADDR
(ALL)
System Reset
SELRS (5)
AINZX (3) (5)
IN (5)
LCMD (2)
CRCEN (4)

Notes:
1. >> To or from disk drive.
2. > Jumper connections.
3. Numbers contained in boxes refer to paragraph and logic location.
4. Numbers in parenthesis identify a logic block in figure 3-1 as the source or destination of the indicated signal(s). Figures showing logic within each block are as follows:
   - Block 1, Processor Interface: figure 3-2, page 3-3
   - Block 2, DMA Control: figure 3-3, page 3-7
   - Block 3, Control Function: figure 3-5, page 3-15
   - Block 4, Read/Write Function: figure 3-6, page 3-24
   - Block 5, Disc Control and Interface: figure 3-7, page 3-30

Figure 3-2. Processor Interface (1)

3.2.1.7 Status Reset

The Status Reset logic causes certain status associated flags to be reset upon execution of an Input command by the disk controller, or when the system reset (RST) signal is active. The following flags and counter are reset by the logic:

PHALT	RATER	DACCE	(Mnemonic description
SCD0 thru SCD3 thru	HAERF	EOC	provided in appendix A)
Timeout counter			

3.2.1.8 Initializer Logic

The Initializer Logic generates a select restore signal (SELRS) or a command initialized system reset. A processor reset (RST-) also generates a system reset.

3.2.2 Interrupt Function

3.2.2.1 Interrupt Enable

The Interrupt Enable logic enables one interrupt to be initiated by the disk controller. The logic is essentially comprised of two flip-flops: the Interrupt Mask (IMSK) and the Interrupt Mask Reset (IMRS). To enable interrupts, the IMSK flip-flop is set by issuing an Output command with the appropriate device address and a function code of 3. Interrupts are disabled when the IMRS flip-flop is set, which subsequently resets IMSK. This normally occurs after the interrupt address is sent to the Processor in response to an interrupt address request from the Processor (IAR).

3.2.2.2 Interrupt Stimulus Store

The Interrupt Stimulus Store logic stores the fact that the disk controller is requesting an interrupt. PHALT causes an interrupt pending condition to occur (INTS). The PHALT flip-flop is set when a controller reset (CONRS) occurs indicating the controller is finished with the operation being performed. The PHALT flip-flop is cleared when status is input to the Processor to determine the cause of the interrupt.

3.2.2.3 Interrupt Pending

The Interrupt Pending logic synchronizes interrupt requests to Processor timing. The logic is essentially comprised of the INTS flip-flop which is set when the Interrupt Stimulus Store logic is active (PHALT), or one of the four seek complete flip-flops (SCD0 thru SCD3) is set and the controller is idle. INTS being set will initiate an interrupt if interrupts are enabled, and the disk controller has interrupt priority.

3.2.2.4 Interrupt Request

The Interrupt Request logic initiates the interrupt by sending the IUR signal to the Pr
cessor if an interrupt is pending (INTS), interrupts are enabled (IMSK), and the dis
controller has interrupt priority (PRIN).

3.2.2.5 Interrupt Address Encoder

The Interrupt Address Encoder encodes and transmits the interrupt address to the Pr
cessor in response to an interrupt address request (IAR) from the Processor. The ba
interrupt address associated with the disk controller is : 000. This has been offset to
"standard" interrupt address of : 00A by rear-edge connector (J11) jumpering on the
board. This standard address can be changed if necessary. Refer to paragraph 2.17

3.2.2.6 Interrupt Priority

The Interrupt Priority logic passes priority (PROT) to down-stream devices if it is av
able to the disk controller, and the disk controller is not using it. Priority is control
by the Interrupt Request logic (ME). If the Interrupt Request logic is active, priority
will not be relinquished to down-stream devices until the interrupt request has been
viced.

3.2.3 DMA Control Function (Figure 3-3)

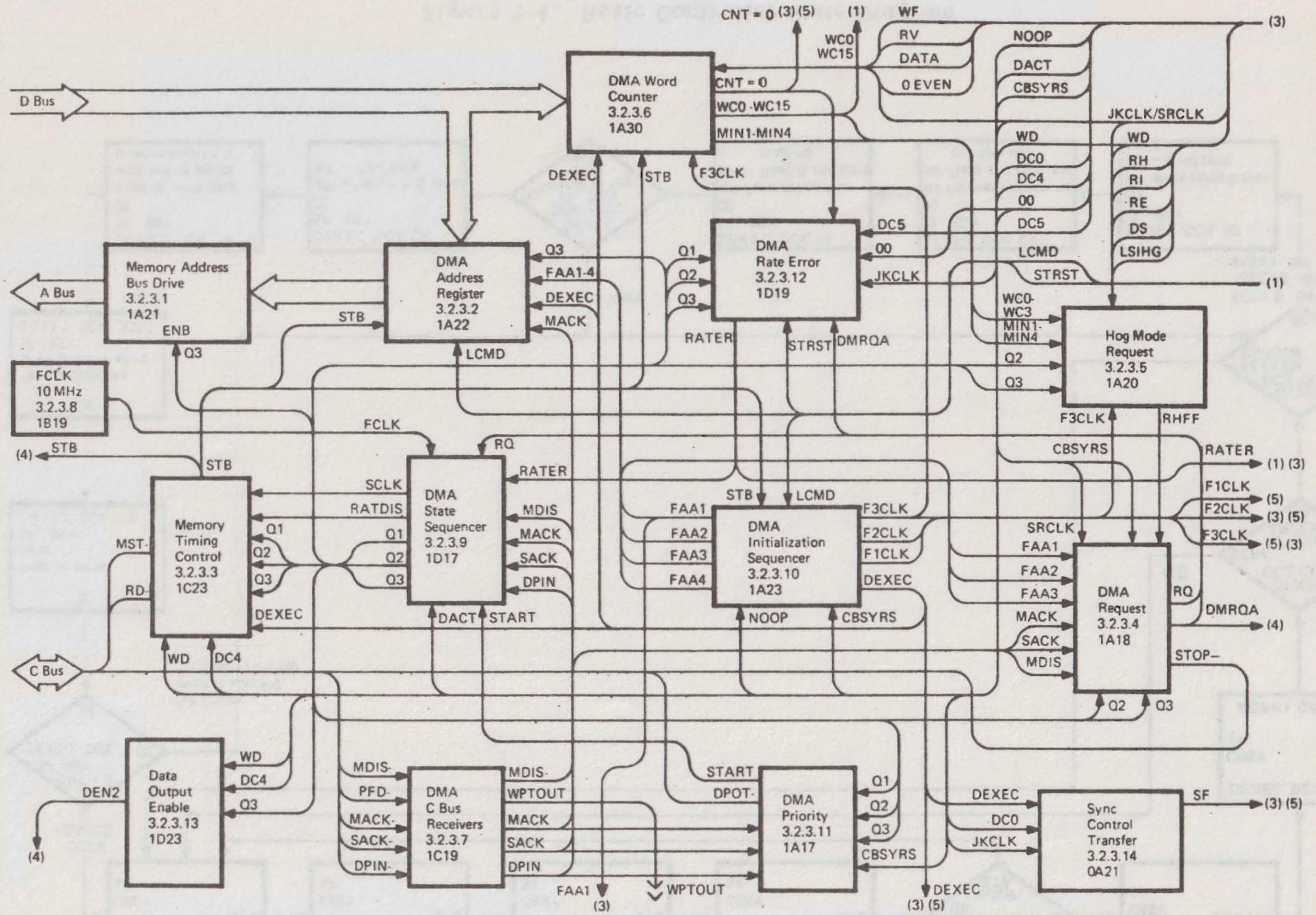
Refer to the DMA state diagram in figure 3-4 for state changes associated with the DM
Control Function.

3.2.3.1 Memory Address Bus Drivers

The Memory Address Bus Drivers apply the contents of the DMA Address Register to Address (A) bus lines 0 thru 14 when enabled by the DMA State Sequencer (3.2.3.9) being in Q3 time.

3.2.3.2 DMA Address Register

The DMA Address Register is a 15-bit down-counter which stores the address (in one
complement) of the location in Memory from which data is to be extracted (Write Oper
or stored (Read operation). The address in the register is automatically incremented
the end of each DMA cycle to provide access to the next sequential location in the Dat


D Bus
A Bus
C Bus
DMA Word Counter 3.2.3.6 1A30
CNT = 0 (3) (5)
(1)
WC0 WC15
WF
RV
DATA
0 EVEN
CNT = 0
WC0-WC15
MIN1-MIN4
DEXEC
STB
F3CLK
NOOP
DACT
CBSYRS
JKCLK/SRCLK
(3)
WD
DC0
DC4
00
DC5
LCMD
STRST
WD
RH
RI
RE
DS
LSIHG
(1)
Memory Address Bus Drive 3.2.3.1 1A21
ENB
Q3
DMA Address Register 3.2.3.2 1A22
Q3
FAA1-4
DEXEC
MACK
STB
LCMD
DMA Rate Error 3.2.3.12 1D19
Q1
Q2
Q3
DC5
00
JKCLK
RATER
STRST
DMRQA
WC0-WC3
MIN1-MIN4
Q2
Q3
Hog Mode Request 3.2.3.5 1A20
F3CLK
RHFF
FCLK 10 MHz 3.2.3.8 1B19
FCLK
(4) STB
STB
RQ
Memory Timing Control 3.2.3.3 1C23
MST-
RD-
SCLK
RATDIS
Q1
Q2
Q3
Q1
Q2
Q3
DEXEC
WD
DC4
DMA State Sequencer 3.2.3.9 1D17
RATER
MDIS
MACK
SACK
DPIN
DACT
START
STB
LCMD
DMA Initialization Sequencer 3.2.3.10 1A23
FAA1
FAA2
FAA3
FAA4
F3CLK
F2CLK
F1CLK
DEXEC
NOOP
CBSYRS
CBSYRS
RATER
(1) (3)
F1CLK
(5)
F2CLK
(3) (5)
F3CLK
(5) (3)
SRCLK
FAA1
FAA2
FAA3
MACK
SACK
MDIS
DMA Request 3.2.3.4 1A18
RQ
DMRQA
(4)
STOP-
Q2
Q3
Data Output Enable 3.2.3.13 1D23
DEN2
(4)
WD
DC4
Q3
MDIS-
PFD-
MACK-
SACK-
DPIN-
DMA C Bus Receivers 3.2.3.7 1C19
MDIS-
WPTOUT
MACK
SACK
DPIN
FAA1
(3)
WPTOUT
START
DPOT-
DMA Priority 3.2.3.11 1A17
Q1
Q2
Q3
CBSYRS
DEXEC
(3) (5)
DEXEC
DC0
JKCLK
Sync Control Transfer 3.2.3.14 0A21
SF
(3) (5)

Notes:
1. >> To or from disk drive.
2. > Jumper connections.
3. Numbers contained in boxes refer to paragraph and logic location.
4. Numbers in parenthesis identify a logic block in figure 3-1 as the source or destination of the indicated signal(s). Figures showing logic within each block are as follows:
    - Block 1. Processor Interface: figure 3-2, page 3-3
    - Block 2. DMA Control: figure 3-3, page 3-7
    - Block 3. Control Function: figure 3-5, page 3-15
    - Block 4. Read Write Function: figure 3-6, page 3-24
    - Block 5. Disc Control and Interface: figure 3-7, page 3-30

Figure 3-3. DMA Control Function (2)

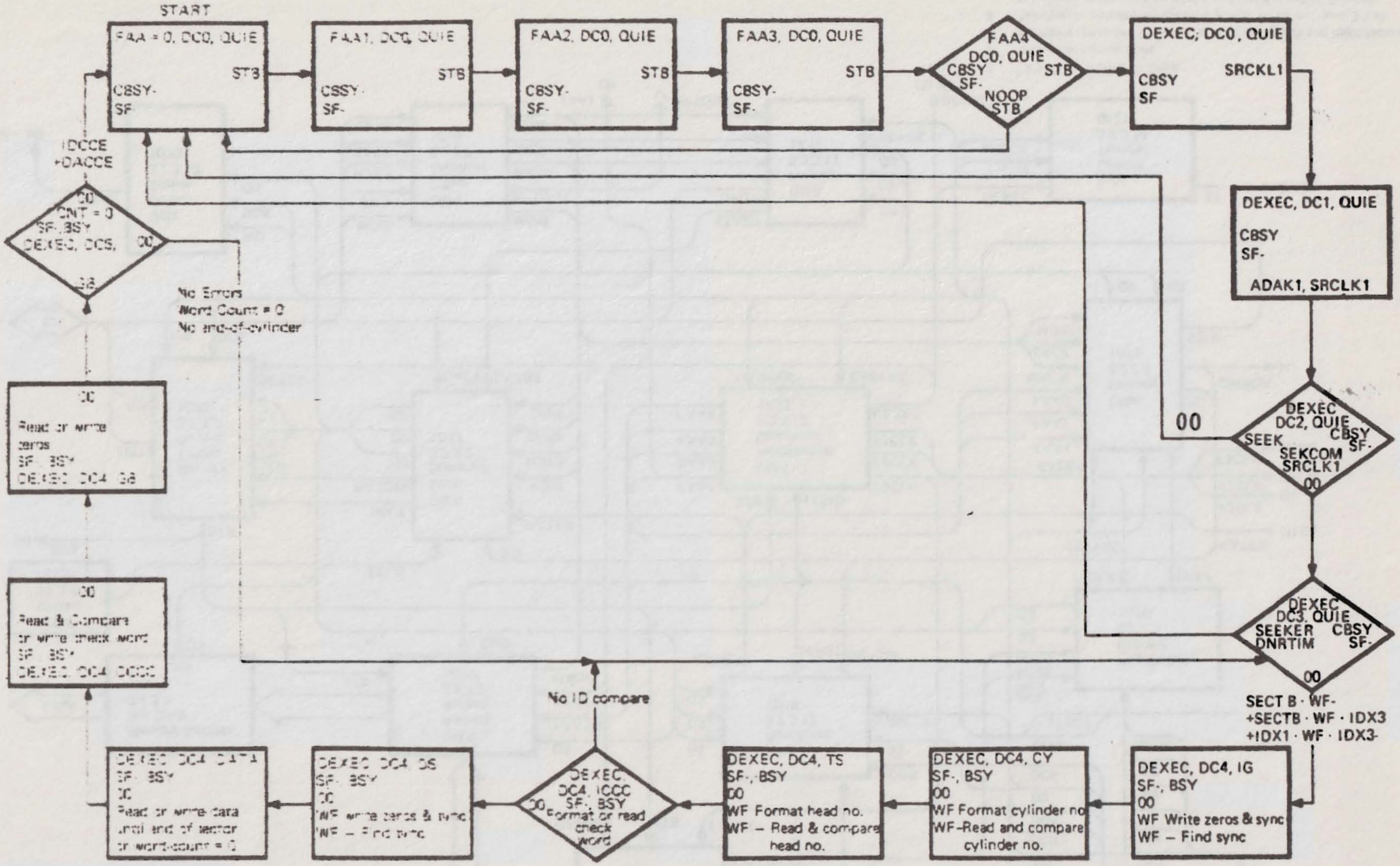

START
FAA = 0, DC0, QUIE
STB
CBSY-
SF
FAA1, DC0, QUIE
STB
CBSY-
SF-
FAA2, DC0, QUIE
STB
CBSY-
SF-
FAA3, DC0, QUIE
STB
CBSY-
SF-
FAA4
DC0, QUIE
CBSY
SF-
STB
NOOP
STB
DEXEC; DC0, QUIE
CBSY
SF
SRCKL1
DEXEC, DC1, QUIE
CBSY
SF-
ADAK1, SRCLK1
00
DEXEC
DC2, QUIE
SEEK
CBSY
SF-
SEKCOM
SRCLK1
00
DEXEC
DC3, QUIE
SEEKER
DNRTIM
CBSY
SF-
00
SECT B · WF-
+SECTB · WF · IDX3
+IDX1 · WF · IDX3-
DEXEC, DC4, IG
SF-, BSY
00
WF Write zeros & sync
WF – Find sync
DEXEC, DC4, CY
SF-, BSY
00
WF Format cylinder no
WF–Read and compare cylinder no.
DEXEC, DC4, TS
SF-, BSY
00
WF Format head no.
WF – Read & compare head no.
No ID compare
DEXEC
DC4, ICCC
SF-, BSY
Format or read check word
00
DEXEC DC4 DS
SF- BSY
00
WF write zeros & sync
WF – Find sync
DEXEC DC4 DATA
SF- BSY
00
Read or write data until end of sector or word-count = 0
00
Read & Compare or write check word
SF- BSY
DEXEC DC4 DCCC
00
Read or write zeros
SF- BSY
DEXEC DC4 GB
00
CNT = 0
SF-,BSY
DEXEC, DC5,
00
GB
IDCCE
+DACCE
No Errors
Word Count = 0
No end-of-cylinder

Figure 3-4. Basic Controller State Diagram

field during the next DMA cycle. The starting address of the Data field (contained in word four of the four-word Disk Control block) is loaded into the DMA Address Register directly after memory acknowledge (MACK) occurs. This will be during FAA4 (fourth word) and during Q3 time. (Refer to figure 3-4).

The DMA Address Register is also used for accessing the four words of the Disk Control block from Memory. The starting address of the Disk Control block is loaded into the DMA Address Register when the Output command which initiates a disk operation is executed (LCMD).

3.2.3.3 Memory Timing Controls

The Memory Timing Controls accept inputs from the DMA State Sequencer to produce Memory control signals during DMA cycles. Signal STB is used as a strobe throughout the controller.

3.2.3.4 DMA Request

The DMA Request logic accepts inputs from various portions of the disk controller to produce requests for DMA cycles at the appropriate times. The Stop Request (STOP) is sent to the Processor whose response is a STOP Acknowledge (SACK) signal when it relinquishes control of Memory to the disk controller. DMA requests are normally made after a data word has been written on, or read from, the selected disk; or when a word (16 bits) has been read from the Identifier field of a sector during the Read Identifier command. During acquisition of the Disk Control block from Memory, output signals from the DMA Initialization Sequencer (FAA1 thru 3) keep the STOP Request continuously true so it will not relinquish Memory control to the Processor until all four words have been extracted. This provides DMA in the "burst" mode which also occurs during Read Data operations in the "hog mode".

3.2.3.5 Hog Mode Request

The Hog Mode Request logic is essentially comprised of a flip-flop which is set when a Read Data operation in the Hog Mode (RH) is to be performed. The output of the flip-flop keeps the DMA request active so it will not relinquish Memory control to the Processor. This ensures the fastest possible transfer rate. When the controller is installed in a Type I processor the Hog Mode is always used during data transfer.

3.2.3.6 DMA Word Counter

The DMA Word Counter keeps track of the number of words transferred during a data transfer operation (Read or Write Data). The number of words to be transferred is contained in the third word of the Disk Control block and is loaded directly (in one's complement) from the D bus. The counter is decremented once for each word transferred (STB) and the operation ceases when the word count is equal to zero (FFFF in one's complement).

The DMA Word Counter also keeps track of the number of sectors to be formatted during a Write Format operation, or the number of sectors to be verified during a Read Verify operation. This is done by loading the counter with a word count equal to the number of sectors to be formatted or verified, times the number of words in the Data field of each sector. (Word count is contained in Word 3 of Disk Control block.) The counter is decremented once for each 16-bit time (one word time) as decoded from the contents of Bit/Byte Counter (0EVEN signal). Thus, after the designated number of words have been counted, the DMA Word Counter will equal zero (CNT =0) and the operation will terminate.

3.2.3.7 DMA C Bus Receivers

The DMA C Bus Receivers buffer the DMA related control lines.

3.2.3.8 FCLK Generator

The FCLK Generator produces a free running 10 MHZ clock for use in the DMA State Sequencer.

3.2.3.9 DMA State Sequencer

The DMA State Sequencer steps the DMA Control Function portion of the disk controller through a DMA cycle. It is enabled when the Processor responds to a STOP request with a STOP acknowledge (SACK). Conditions occurring during the various states of the sequencer are listed below.

STATE			CONDITION
Q3	Q2	Q1	
0	0	0	Quiesent state. No DMA cycle.
0	0	1	
0	1	1	Reset START and REQ flip-flops at the leading edge of Q2.
1	1	1	Place contents of DMA Address Register on A Bus. The period between SACK and the leading edge of Q3 allows time for DMA priority (DPIN) ripple.
1	1	0	1. Memory Start (MST). Wait for MACK. 2. Enable Memory Read (RD) if reading from memory (Write Data operation or loading Disk Control block). Enable Data Output (DEN2) if writing into memory. 3. When MACK occurs advance to next state and set REQ if in the "Hog Mode".
1	0	0	Generate data strobe (STB) at end of Q3 which does the following:
	to		
0	0	0	1. Generates F1CLK, F2CLK, or F3CLK depending on state of DMA Initialization Sequencer. 2. Increments DMA Initialization Sequencer on trailing edge. 3. Decrements DMA Word Counter (trailing edge) if in final state of DMA Initialization Sequencer (DEXEC) and in a data transfer operation (Read or Write Data). 4. Increments DMA Address Register (trailing edge) if in any state of DMA Initialization Sequencer except quiesent state (all outputs "0") or if the fourth word of the control block is being requested from memory (FAA4). 5. Load Write Buffer if Write Data operation.
0	0	0	1. Enable DMA priority (DPOT-) to be passed on to down-stream devices. 2. Disable Memory Address Bus Drivers.

3.2.3.10 DMA Initialization Sequencer

The DMA Initialization Sequencer controls the disk controller while extracting the four-word Disk Control Block from Memory. The sequencer is initialized by LCMD from the I/O Command logic and is incremented by STB each time the DMA State Sequencer cycle The Disk Control Block is extracted from Memory in the "burst" mode during FAA1, FA and FAA3. Conditions which occur during the states of the sequencer are listed below.

STATE	CONDITION
FAA1	1. Request first DMA cycle. (Set RQ.) 2. Start Timeout Counter. 3. Initial Sync Reset if platter change (RS2). 4. First DMA cycle takes place. At the end of Q3 time, load head and sector addresses into Head (TR)/Sector register (trailing edge of F1CLK signal). 5. Request second DMA cycle. (FAA1 keeps RQ true beyond the leading edge of MACK causing REQ to set again.)
FAA2	1. Second DMA cycle takes place. At the end of Q3 time, load cylinder and unit addresse and command into Cylinder, Unit Select an Disk Command registers respectively (Tra ing edge of F2CLK signal). 2. Initiate Sync Reset if drive change (RS2). 3. Request third DMA cycle.
FAA3	1. Third DMA cycle takes place. At the end c Q3 time, load word count into DMA Word Counter and set disk controller to busy status if any command other than NOOP (trailing edge of F3CLK signal). 2. Clear RS2 if set during FAA2. 3. Request fourth DMA cycle.

FAA4	1.	Fourth DMA cycle takes place. At the start of MACK, load starting address of Memory Data field into DMA Address Register. The leading edge of STB resets the DMA Initialization Sequencer to zero if NOOP command is contained in Disk Command Register.
DEXEC	1.	Place controller in "execute" state. a. Disable further stepping of DMA Initialization Sequencer. b. Enable Sync Control Transfer logic to transfer control of disk controller to Disk Control Counter (SF signal causes Disk Control Counter to increment to DC1).

3.2.3.11 DMA Priority

The DMA Priority logic passes DMA priority on to down-stream devices it if is available to the disk controller, and the disk controller is not using it. DMA priority is inhibited from down-stream devices from the time the STOP acknowledge signal (SACK) is received until the end of Q3.

3.2.3.12 DMA Rate Error

The DMA Rate Error logic indicates a rate error (RATER) if a DMA cycle is being requested (DMARQA signal) while a previously requested DMA cycle has not yet occurred or is still cycling.

3.2.3.13 Data Output Enable

The Data Output Enable logic enables (DEN2) the D Bus Drivers in the Read/Write Function to place the contents of the Read Buffer onto the D bus during Q3 of a DMA cycle originated during a Read operation (WD-).

3.2.3.14 Sync Control Transfer

The Sync Control Transfer logic is essentially comprised of one flip-flop (SF) which is set on the first bit-time clock pulse (JKCLK) after the DMA Initialization Sequencer reaches the DEXEC state. The flip-flop remains set for one bit period. The SF signal going true causes the Disk Control (DC) Counter to be incremented to DC1, thereby transferring control of the disk controller to the Disk Control (DC) Counter. It also causes the following to occur on its trailing edge:

1. Load head address (contained in Head Sector Register) into Head Select Register. (Head Select Register is only used with maximum of four heads.)
2. Enable detection of head address error (addressed head greater than maximum numbered head).

3.2.4 Control Function (Figure 3-5)

3.2.4.1 Read Clock Synchronizer

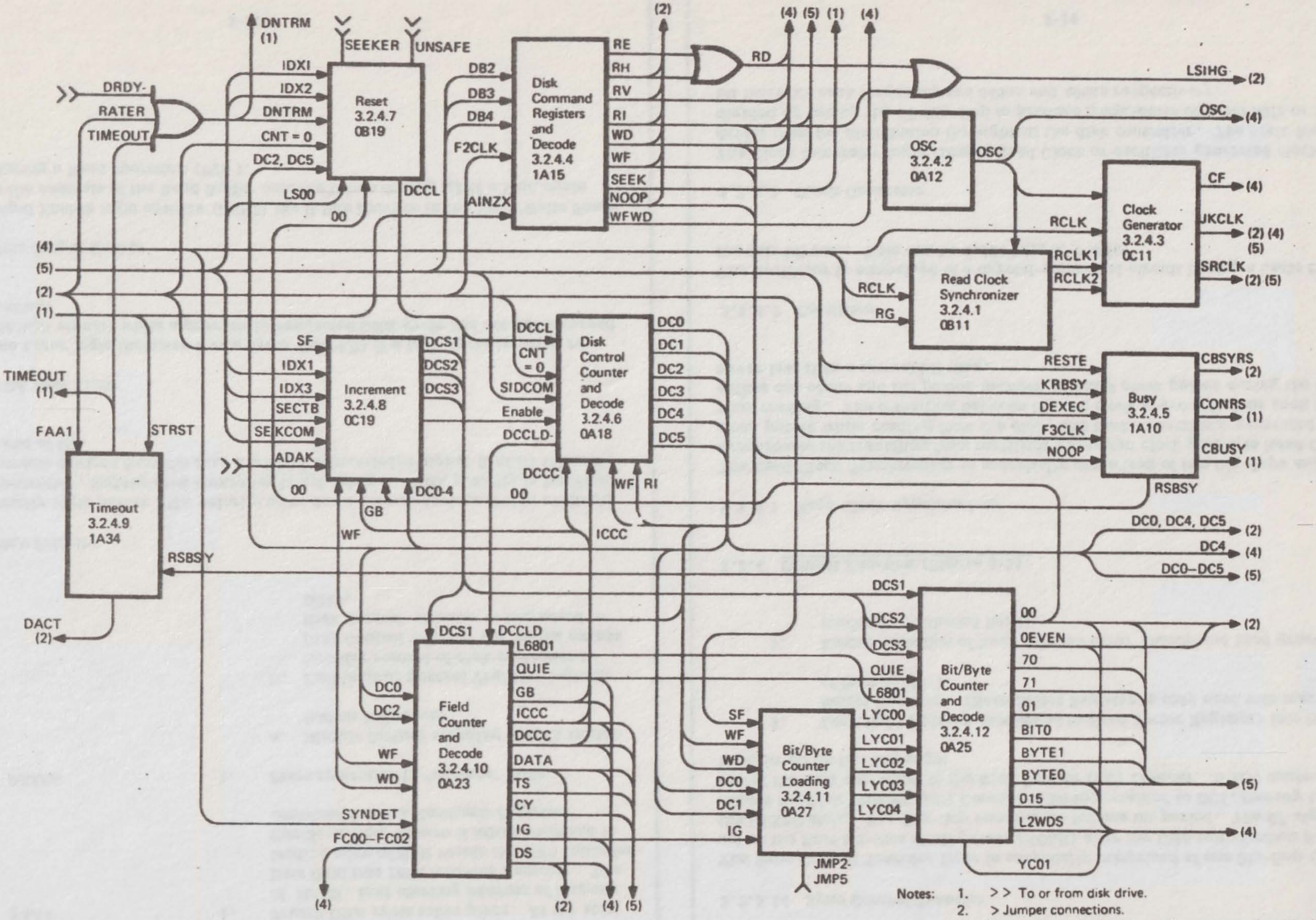
The Read Clock Synchronizer is essentially comprised of two flip-flops and is used to synchronize the transition from oscillator generated clock pulses to Read Clock generated clock pulses while reading from the disk, and back to oscillator generated clock pulses after reading. The transition between the two clock sources is done such that no clock spikes can occur and the period between adjacent clock pulses during the transition is never less than a normal bit time.

3.2.4.2 Oscillator

The Oscillator is comprised of a crystal-controlled circuit having a basic frequency twice the data bit rate. This can be 3.124 MHz or 5 MHz.

3.2.4.3 Clock Generator

The Clock Generator logic accepts Read Clock or oscillator generated clock pulses and drives them for distribution throughtout the disk controller. The basic frequency is divided by two by the CF flip-flop to produce frequencies of 1.562 MHz or 2.5 MHz. The bit times for each frequency are 640ns and 400ns respectively.


DNTRM
(1)
SEEKER
UNSAFE
IDXI
IDX2
DNTRM
CNT = 0
DC2, DC5
LS00
00
DCCL
Reset
3.2.4.7
0B19
DRDY-
RATER
TIMEOUT
DB2
DB3
DB4
F2CLK
AINZX
Disk
Command
Registers
and
Decode
3.2.4.4
1A15
RE
RH
RV
RI
WD
WF
SEEK
NOOP
WFWD
(2)
RD
(4) (5) (1) (4)
LSIHG
(2)
OSC
(4)
OSC
3.2.4.2
0A12
OSC
CF
(4)
Clock
Generator
3.2.4.3
0C11
UKCLK
(2) (4)
(5)
SRCLK
(2) (5)
RCLK
RCLK1
RCLK2
RCLK
RG
Read Clock
Synchronizer
3.2.4.1
0B11
(4)
(5)
(2)
(1)
DCCL
CNT
= 0
SIDCOM
Enable
DCCLD
Disk
Control
Counter
and
Decode
3.2.4.6
0A18
DC0
DC1
DC2
DC3
DC4
DC5
SF
IDX1
IDX3
SECTB
SEKCOM
ADAK
00
Increment
3.2.4.8
0C19
DCS1
DCS2
DCS3
GB
DC0-4
WF
DCCC
00
WF
RI
ICCC
TIMEOUT
(1)
FAA1
STRST
Timeout
3.2.4.9
1A34
RSBSY
DACT
(2)
RESTE
KRBSY
DEXEC
F3CLK
NOOP
Busy
3.2.4.5
1A10
CBSYRS
(2)
CONRS
(1)
CBUSY
(1)
RSBSY
DC0, DC4, DC5
(2)
DC4
(4)
DC0–DC5
(5)
DCS1
DCCLD
L6801
QUIE
GB
ICCC
DCCC
DATA
TS
CY
IG
DS
DC0
DC2
WF
WD
SYNDET
FC00–FC02
Field
Counter
and
Decode
3.2.4.10
0A23
(4)
(2)
(4)
(5)
DCS1
DCS2
DCS3
QUIE
L6801
LYC00
LYC01
LYC02
LYC03
LYC04
SF
WF
WD
DC0
DC1
IG
Bit/Byte
Counter
Loading
3.2.4.11
0A27
JMP2-
JMP5
Bit/Byte
Counter
and
Decode
3.2.4.12
0A25
00
0EVEN
70
71
01
BIT0
BYTE1
BYTE0
015
L2WDS
YC01
(2)
(5)
(4)

Notes:
1. >> To or from disk drive.
2. > Jumper connections.
3. Numbers contained in boxes refer to paragraph and logic location.
4. Numbers in parenthesis identify a logic block in figure 3-1 as the source or destination of the indicated signal(s). Figures showing logic within each block are as follows:
   - Block 1, Processor Interface: figure 3-2, page 3-3
   - Block 2, DMA Control: figure 3-3, page 3-7
   - Block 3, Control Function: figure 3-5, page 3-15
   - Block 4, Read Write Function: figure 3-6, page 3-24
   - Block 5, Disc Control and Interface: figure 3-7, page 3-30

Figure 3-5. Control Function (3)

3.2.4.4 Disk Command Register and Decode

The Disk Command Register and Decode is comprised of three flip-flops which store bits 2, 3, and 4 of Word 2 of the Disk Control Block (command coding) and logic which decodes the contents of the Disk Command Register for all commands. Eight outputs provide overall control of the disk controller as dictated by the type of command being performed.

3.2.4.5 Busy

The Busy logic indicates when the disk controller is busy performing some operation. The CMBSY flip-flop is set by F3CLK for all commands (other than NOOP) which are initiated by the Disk Control block. CBUSY is generated by CMBSY or RSBSY when a Restore command (RESTE) is executed by the controller. The controller goes not busy (idle) upon termination of the operation being performed. In the case of a Seek Only command the controller goes idle when the selected disk drive indicates acceptance of the command (via the ADACK signal) which allows overlapped seeks. The ADACK signal causes the Disk Control Counter to advance to DC2. The occurrence of DC2 and SEEK (seek only) during bit/byte time 00 resets the DC Counter and the controller goes idle. The status of the controller, which is reflected by the CBUSY signal, can be interrogated by Sense command or Status input. The CONRS output signal is used to initiate a program interrupt upon termination of an operation, if interrupts are enabled. Term CBSYRS occurs when the CONRS flip-flop is set or when a system reset occurs.

3.2.4.6 Disk Control Counter and Decode

The Disk Control Counter and Decode assumes control of the disk controller after the four-word Disk Control block has been loaded into the controller (except in the case of the NOOP command). The quiescent state of the counter is DC0. It is incremented to DC1 by the SF signal, controls the cylinder seek operation during DC1 and DC2, and performs the remainder of the operation during DC3, 4, and 5, returning to DC0 upon termination of the operation (Refer to figure 3-4). Three different operations are performed on the Disc Control Counter. It can be preset to three (DCCLD), incremented, or reset (DCCL). The preset to three occurs when there has been no ID compare or after the DC Counter has incremented to DC5, no errors have occurred, the end of the cylinder has not been reached, and the word count is not equal to zero. The DC Counter is reset by DCCL from the Reset logic (3.2.4.7). Incrementing occurs on time with the SRCLK and is enabled by the Increment logic (3.2.4.8).

The decode logic decodes the contents of the Disk Control Counter. Its outputs are listed below, along with a description of each. (Note that this does not apply to the NOOP command.)

COUNT	DESCRIPTION
DC0	Quiescent state.
DC1	Cylinder Seek operation started. The cylinder address is sent to the selected disk drive. If a Diablo disk drive is used, it responds with an Address Acknowledge signal after accepting the address. Otherwise, the signal is held true by rear-edge connector J11 (on 531 board) jumpering. In any case, the signal is synchronized to controller timing and causes the counter to increment to DC2.
DC2	The seek operation is completed in DC2. Upon completion, the controller is notified and the counter is incremented to DC3. If a Seek Only operation is being performed, the counter is reset to DC0.
DC3	A starting point for the Read or Write operation is found. For all operations except Write Format this is the beginning of the first sector encountered. For Write Format, it is the Index pulse which signifies the beginning of the operation. This occurs at the beginning of Sector 0. Upon finding the starting point, the counter is incremented to DC4.
DC4	Reading and writing of information is done in this state. Depending upon the operation being performed, certain events occur. These are listed below: 1. Read or Write Data, Read Verify. The Identifier field is read and compared to the cylinder-head-sector address received from the Disk Control block. If a positive comparison

is made, the operation is performed and the counter is incremented to DC5 at the end of the sector. If no ID comparison is made, the counter is set back to DC3 to await the beginning of the next sector so another ID comparison can be made. If the ID fields in all sectors of a track have been compared and no positive comparison occurs (ID search error), the counter is reset to DC0 and the operation terminates.

2. Write Format. The sector is formatted. This includes writing the ID field (cylinder-head-sector address), the ID field cyclic check word, the Data Sync field, Data field of all zeros, a Data field cyclic check word, and the guard bytes. The counter is incremented to DC5 at the end of the sector.

3. Read ID. The ID field of the first sector encountered is read and sent to Memory. The counter is incremented to DC5 at the end of the sector.

DC5 Provides re-cycle or end-of-operation control at the end of each sector. If the contents of the DMA Word Counter have been decremented to zero, the operation is completed and the counter is reset to DC0. If the word count is not equal to zero and no error conditions have occurred, the counter is set back to DC3 to await the beginning of the next sector to continue the operation. If an error condition has occurred, the counter is reset to DC0.

NOTE

During any disk control count other than DC0 (DC1 thru DC5), the Disk Control Counter will reset to DC0 if an error occurs at the selected disk drive (drive not ready, unsafe, or seek error).

3.2.4.7 Reset

The Reset logic resets the Disk Control Counter by generating term DCCL. The conditions which will cause a reset are listed below:

1. Selected disk drive errors - UNSAFE, SEEKER, DRDY- (disk not ready).
2. Rate Error (RATER).
3. TIMEOUT (See 3.2.4.9).
4. Cyclic check errors (IDCCE, DACCE).
5. Identifier search error (IDX1 and IDX2).
6. Index or sector pulse occurs (INXSCT) during write operation.
7. DC2 and 00 during seek only operation.
8. DC5, last byte/bit (00), last sector (SECCOM), last head (HAERR).
9. DC5 and 00 (DC500) with word count equal to zero (CNT = 0).

3.2.4.8 Increment

The Increment logic enables the Disk Control Counter to increment. The transition of states and the conditions required are listed below. (Refer to figure 3-7).

STATE	CHANGE	CONDITIONS
DC0	DC1	All four words of the Disk Control block have been extracted (SF).
DC1	DC2	Acknowledge from disk (ADACK) and bit/byte count equals zero (00).
DC2	DC3	Seek complete (SEKCOM) and 00.
DC3	DC4	Not in write format (WF-), a sector pulse occurred (SECTB) and 00; or if in write format (WF), an index pulse occurred (IDX1), and 00; or when multiple sector formating (going from

		DC5 to DC3) IDX3 will be set (from the previous DC5) and the occurrence of a sector pulse (SECTB) and 00 will increment the counter.
DC4	DC5	Head is over guard bytes field (GB) and 00 occurs.

3.2.4.9 Timeout

The Timeout logic provides a time period within which any Disk Control block initiated operation must be completed. The logic also times the initiation of Restore operations which must be completed within the same time period. This time period is between 4.62 and 5.28 seconds after the operation is initiated. The timeout period includes the time required to transfer the four word control block.

3.2.4.10 Field Counter and Decode

The Field Counter and Decode keeps track of the particular field of a sector over which the head is presently located. The counter is a modulo 9 counter, counting between 0, the quiescent state, and 8, when the head is over the Guard Bytes field. The counter is incremented to 1 at the beginning of each sector when the Disk Control Counter is incremented to DC4. It is thereafter incremented at the end of each field. The fields of a sector as defined by the Field Counter are not necessarily those described under Sector Format in Section 1 (paragraph 1.3.1, and appendix A under the mnemonics associated with the various fields).

FIELD	DESCRIPTION
QUIE	Quiescent state of Field Counter when not actively processing a sector.
IG	Includes the Sector Gap and Identifier Sync subfields. The former accommodates worst-case read amp recovery after switching heads, or after termination of a write operation. It also allows sufficient time for electrical and mechanical tolerances. The Sector Gap sub-field is also used for synchronizing the Read/Data Clock Recovery logic in the disk controller to the incoming data/clock stream. The Identifier Sync sub-field is used to search for the Sync character (: 7F) which is contained in the last byte of the sub-field and (IG field).
CY	First half of Identifier field. Contains cylinder address.
TS	Second half of Identifier field. Contains head and sector address.
ICCC	Contains Identifier field cyclic check word.
DS	Data Sync field which is used for sychronizing the Read Data/Clock Recovery logic to the incoming data/clock stream.
DATA	Data field which contains the stored data.
DCCC	Contains Data field cyclic check word.
GB	Guard Bytes field which is necessary to ensure no noise spike will occur in Data Cyclic Check Word field.

3.2.4.11 Bit/Byte Counter Loading

The Bit/Byte Counter Loading logic sets up the appropriate inputs to the Bit/Byte Counter prior to parallel loading. The inputs are always set up in the previous field (field as defined by Field Counter, not Sector Format). The Bit/Byte Counter is then preset to this count at the end of the previous field when the Field Counter is incremented. The loading logic accepts inputs from the Words per Sector strapping input, the Command Register, the Disk Control and Field Counters, the Sync Control Transfer logic, as well as itself (LD1-LD8) to set up the appropriate preset counts at the appropriate times. (Refer to table 3-1).

Table 3-1. Bit/Byte Counter Loading Format

DISK CONTROL COUNTER	FIELD COUNTER	PRESET SIGNALS	BIT/BYTE COUNTER YCO 8 7 6 5 4 3 2 1 0	BCO 3 2 1	BYTES LOADED
DC0	-	-	-		-
DC1	-	LD2, LD4, LD8	1 1 1 1 1 1 1 0 1	0 0 0	3
DC2	-	LD1, LD4, LD8	1 1 1 1 1 1 1 1 1	0 0 0	1
DC3	-	LD1, LD4, LD8	1 1 1 1 1 1 1 1 1	0 0 0	1
DC4	IG (Write Format)	LD5, LD7	1 1 1 0 1 1 0 0 0	0 0 0	40
	IG (Write Format-)	LD6, LD7	1 1 1 1 0 1 0 0 0	0 0 0	24
	CY	LD2, LD4, LD8	1 1 1 1 1 1 1 1 0	0 0 0	2
	TS	LD2, LD4, LD8	1 1 1 1 1 1 1 1 0	0 0 0	2
	ICCC	LD2, LD4, LD8	1 1 1 1 1 1 1 1 0	0 0 0	2
	DS (Write Format or Write Data)	LD4	1 1 1 1 0 0 0 0 0	0 0 0	32
	DS (Write Format or Write Data-)	LD3, LD4, LD8	1 1 1 1 0 1 1 1 0	0 0 0	18
	DATA	JMP5	1 0 0 0 0 0 0 0 0	0 0 0	256
	DATA Determined by Words	JMP4	0 1 0 0 0 0 0 0 0	0 0 0	384
	DATA per Sector assignment	JMP3	0 0 1 0 0 0 0 0 0	0 0 0	448
	DATA (rear-edge connector	JMP2	0 0 0 1 0 0 0 0 0	0 0 0	480
	DATA J11 strapping)	-	0 0 0 0 0 0 0 0 0	0 0 0	512
	DCCC	LD2, LD4, LD8	1 1 1 1 1 1 1 1 0	0 0 0	2
	GB	LD2, LD4, LD8	1 1 1 1 1 1 0 0 0	0 0 0	8
DC5	-	-	-		-
			Byte Counter	Bit Ctr	

3.2.4.12 Bit/Byte Counter and Decode

The Bit/Byte Counter and Decode determines the length of the various fields of each sector while performing the Write Format operation. The counter is loaded with the 2's complement of the number of bits (number of bytes times eight) associated with each field each time the Field Counter is incremented (L6801). It is then incremented by one for each bit time until it contains all "1"s which indicates the end of the field (00 output counter true). The counter is then loaded with the 2's complement of the appropriate number of bits for the next field and the cycle is repeated. This all occurs during DC4 time of the Disk Control Counter.

During DC4 time when performing a Read or Write operation, the counter determines the length of all fields except when reading the IG and DS fields. These fields end when the Sync character (hex : 7F) is detected by the Sync Character Detect logic of the Read/Write Function. A count is used for these fields, however, to approximately indicate the halfway point of the fields for other purposes. The count stays at maximum (all "1"s) until the beginning of the next field.

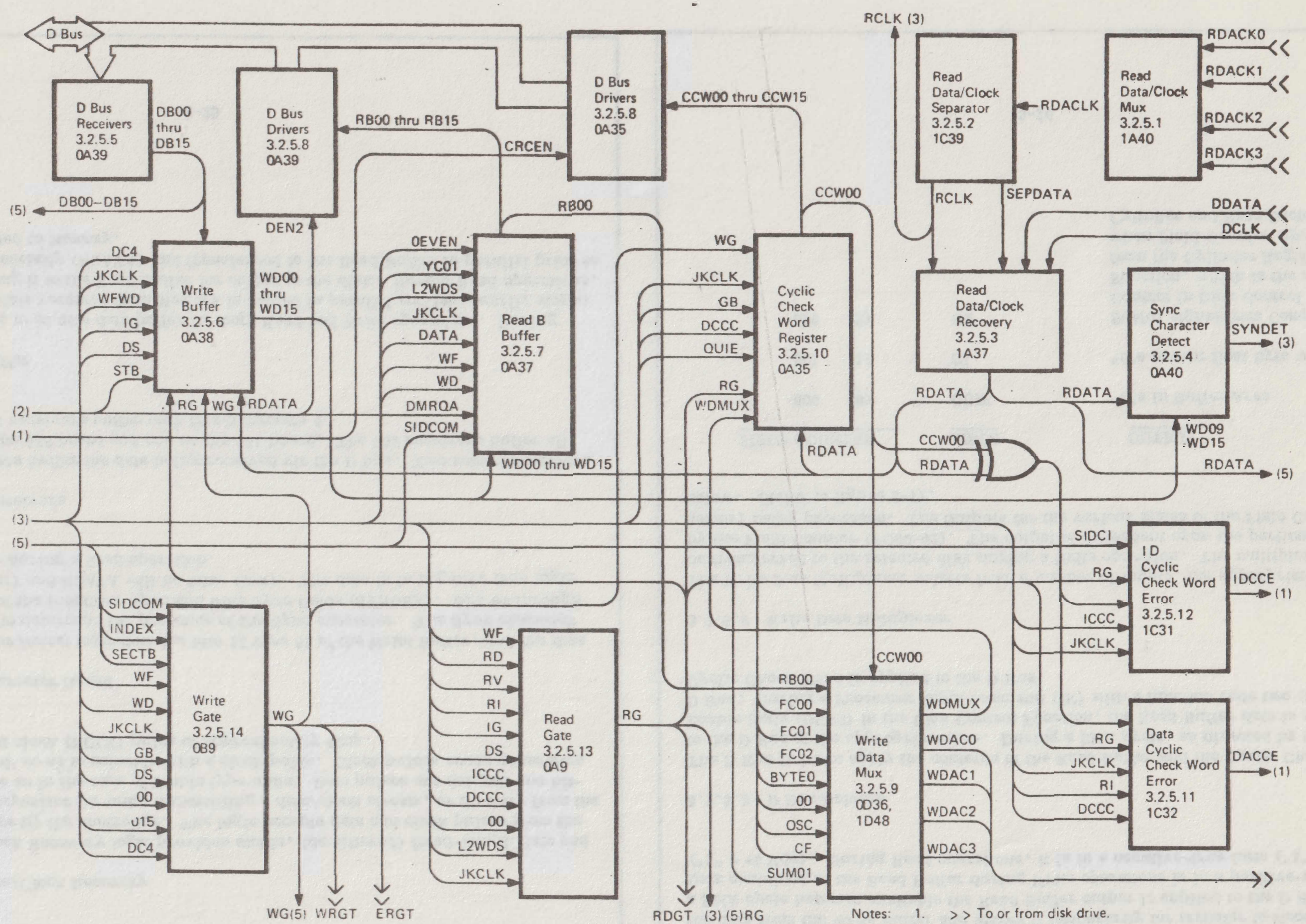
The Bit/Byte Counter is also used during DC1, 2, and 3 for various purposes which are explained in the theory of operation for each function which immediately follows the block diagram description. The loading occurs whenever the Disk Control Counter is incremented except during the transition from DC4 to DC5.

The decode logic decodes the contents of the Bit/Byte Counter to produce various control signals required by the controller. A description of each signal can be found in Appendi A at the rear of the manual.

3.2.5 Read/Write Function (Figure 3-6)

3.2.5.1 Read Data/Clock Multiplexer

The Read Data/Clock Multiplexer accepts the Read Data Clock stream input from all on-line disk drives and outputs only that which is related to the selected unit. The multiplexer is only used if the on-line disk drives are of the type which transmit a data/clock stream.


D Bus
D Bus Receivers 3.2.5.5 0A39
DB00 thru DB15
D Bus Drivers 3.2.5.8 0A39
RB00 thru RB15
CRCEN
D Bus Drivers 3.2.5.8 0A35
CCW00 thru CCW15
RCLK (3)
Read Data/Clock Separator 3.2.5.2 1C39
RDACLK
Read Data/Clock Mux 3.2.5.1 1A40
RDACK0
RDACK1
RDACK2
RDACK3
(5)
DB00–DB15
DEN2
RB00
CCW00
RCLK
SEPDATA
DDATA
DCLK
DC4
JKCLK
WFWD
IG
DS
STB
Write Buffer 3.2.5.6 0A38
WD00 thru WD15
RG
WG
RDATA
0EVEN
YC01
L2WDS
JKCLK
DATA
WF
WD
DMRQA
SIDCOM
Read B Buffer 3.2.5.7 0A37
WD00 thru WD15
WG
JKCLK
GB
DCCC
QUIE
RG
WDMUX
Cyclic Check Word Register 3.2.5.10 0A35
RDATA
Read Data/Clock Recovery 3.2.5.3 1A37
Sync Character Detect 3.2.5.4 0A40
SYNDET
(3)
RDATA
RDATA
WD09 WD15
CCW00
RDATA
RDATA
(5)
(2)
(1)
(3)
(5)
SIDCOM
INDEX
SECTB
WF
WD
JKCLK
GB
DS
00
015
DC4
Write Gate 3.2.5.14 0B9
WG
WF
RD
RV
RI
IG
DS
ICCC
DCCC
00
L2WDS
JKCLK
Read Gate 3.2.5.13 0A9
RG
SIDCI
RG
ICCC
JKCLK
ID Cyclic Check Word Error 3.2.5.12 1C31
IDCCE
(1)
CCW00
RB00
FC00
FC01
FC02
BYTE0
00
OSC
CF
SUM01
Write Data Mux 3.2.5.9 0D36, 1D48
WDMUX
WDAC0
WDAC1
WDAC2
WDAC3
RG
JKCLK
RI
DCCC
Data Cyclic Check Word Error 3.2.5.11 1C32
DACCE
(1)
WG(5)
WRGT
ERGT
RDGT
(3) (5)RG

Notes:
1. >> To or from disk drive.
2. > Jumper connections.
3. Numbers contained in boxes refer to paragraph and logic location.
4. Numbers in parenthesis identify a logic block in figure 3-1 as the source or destination of the indicated signal(s). Figures showing logic within each block are as follows.
   Block 1, Processor Interface: figure 3-2, page 3-3
   Block 2, DMA Control: figure 3-3, page 3-7
   Block 3, Control Function: figure 3-5, page 3-15
   Block 4, Read Write Function: figure 3-6, page 3-24
   Block 5, Disc Control and Interface: figure 3-7, page 3-30

Figure 3-6. Read/Write Function (4)

3.2.5.2 Read Data/Clock Separator

The Read Data/Clock Separator logic accepts the Read Data/Clock stream from the selected disk drive and separates the data from the clock information. The separator is only used if the selected disk drive is of the type which transmits a data/clock stream.

3.2.5.3 Read Data/Clock Recovery

The Read Data/Clock Recovery logic provides stable, (de-jittered) fixed-length data and clock pulses for use by the controller. The logic accepts data and clock pulses from the Read Data/Clock Separator for units transmitting a data/clock stream, or directly from the selected disk drive as in the case of Diablo type units. Data pulses are delayed one bit-time and "stretched' so as to coincide with a clock pulse. Clock pulses cause generation of a stabilized read clock (RCLK) pulse of approximately 62ns.

3.2.5.4 Sync Character Detect

The Sync Character Detect logic decodes bits 15 thru 09 of the Write Buffer, and the data bit just received, to determine the presence of the Sync character. The Sync character indicates the end of the Identifier Sync and Data Sync fields (SYNDET). Bits 09 through 15 will be true (low) and RDATA will be false (low). The data is in negative true logic in the Write Buffer during a Read operation.

3.2.5.5 D Bus Receivers

The D Bus Receivers buffer the data being received via the D bus. Two sets of receivers are used, one on the 530 board and one on the 531 board. The 530 receivers buffer all 16 bits and the 531 receivers buffer only bits 0 through 4.

3.2.5.6 Write Buffer

The Write Buffer is used as a data buffer for both Read and Write operations. During Write operations, data received from Memory is loaded in parallel and temporarily stored prior to transferring it to the Read Buffer for output to the disk. During Read operations, the data is loaded serially (RDATA) and transferred to the Read Buffer in parallel prior to its being transferred to Memory.

3.2.5.7 Read Buffer

The Read Buffer is used during both Read and Write operations. During Write operations, it receives the data in parallel form from the Write Buffer and shifts it out serially (RB00) to the Write Data Mux for output to the selected disk. During Read operations, it receives the data from the Write Buffer and stores it temporarily for transfer to Memory. When a DMA cycle becomes available the Read Buffer output is applied to the D Bus Drivers. Data contained in the Read Buffer during Write operations is in a positive-true form ("1" = +5 Vdc). During Read operations, it is in a negative-true form ("1" = 0 Vdc).

3.2.5.8 D Bus Drivers

The D Bus Drivers apply the contents of the Read Buffer and the Cyclic Check Word Regist to the D Bus at the appropriate time. During a DMA cycle, as directed by the Data Output Enable logic (DEN2) in the DMA Control Function, the Read Buffer data is applied to the D Bus. During a Processor input command (IN) with a function code two (CRCEN) the Cyclic Check Word is applied to the D Bus.

3.2.5.9 Write Data Multiplexer

The Write Data Multiplexer selects from a number of inputs, the appropriate information to be transferred to the selected disk during a Write operation. The multiplexer is controlle by the Field Counter (FC00-02). The output is dependent upon the particular field (of a sector) being processed. The Outputs for the various states of the Field Counter are liste below. (Refer to figure 3-7).

FIELD COUNTER		FIELD	OUTPUT
000	(0)	QUIE	"0"s in Buffer Area
001	(1)	IG	"0"s except final byte which is : 7F.
010	(2)	CY	SUM01 signal from Comparison Loop Control in Disk Control and Interface Function, which is the serial output from the Cylinder Register (CF00) when Field Counter equals 2. The Cylinder and Head Sector Registers

			are rotated during Field Count 2 and 3 for updating the Sector and Head addresses when required, and also for outputting to the disk during Write Format operations.
011	(3)	TS	SUM01 signal which is the serial output of the Head Sector registers (CF00) when Field Counter equals 3.
100	(4)	ICCC	CCW00 signal from Cyclic Check Word Register which is serially shifted out to record the cyclic check word associated with the Identifier field.
101	(5)	DS	"0"s except for final byte which is : 7F.
110	(6)	DATA	Serial data from Read Buffer (RB00).
111	(7)	DCCC	CCW00 signal from Cyclic Check Word Register which is serially shifted out for recording the cyclic check word associated with the Data field.
000	(8)	GB	"0"s. (Same as QUIE.)

3.2.5.10 Cyclic Check Word Register

The 16-bit Cyclic Check Word (CCW) Register generates even parity cyclic check words for both the Identifier and Data Fields while writing in these fields. The contents of the register are then recorded in the Identifier or Data Cyclic Check Word field, respectively. When reading the information from these fields, cyclic check words are regenerated from the received data and then compared to the contents of the Identifier or Data Cyclic Check Word field. The two must compare or an error has occurred.

The cyclic check word is an even parity summary of all "1" bits written in the associated field. For example, if the "1" bits written in the bit 0 position of all the words written in the associated field end up being odd, a "1" bit is written in the bit 0 position of the cyclic check word. Likewise, if the "1" bits for the 0 position end up even, a "0" is written in bit position 0 of the cyclic check word. The example below shows a three word Data field with the associated cyclic check word.

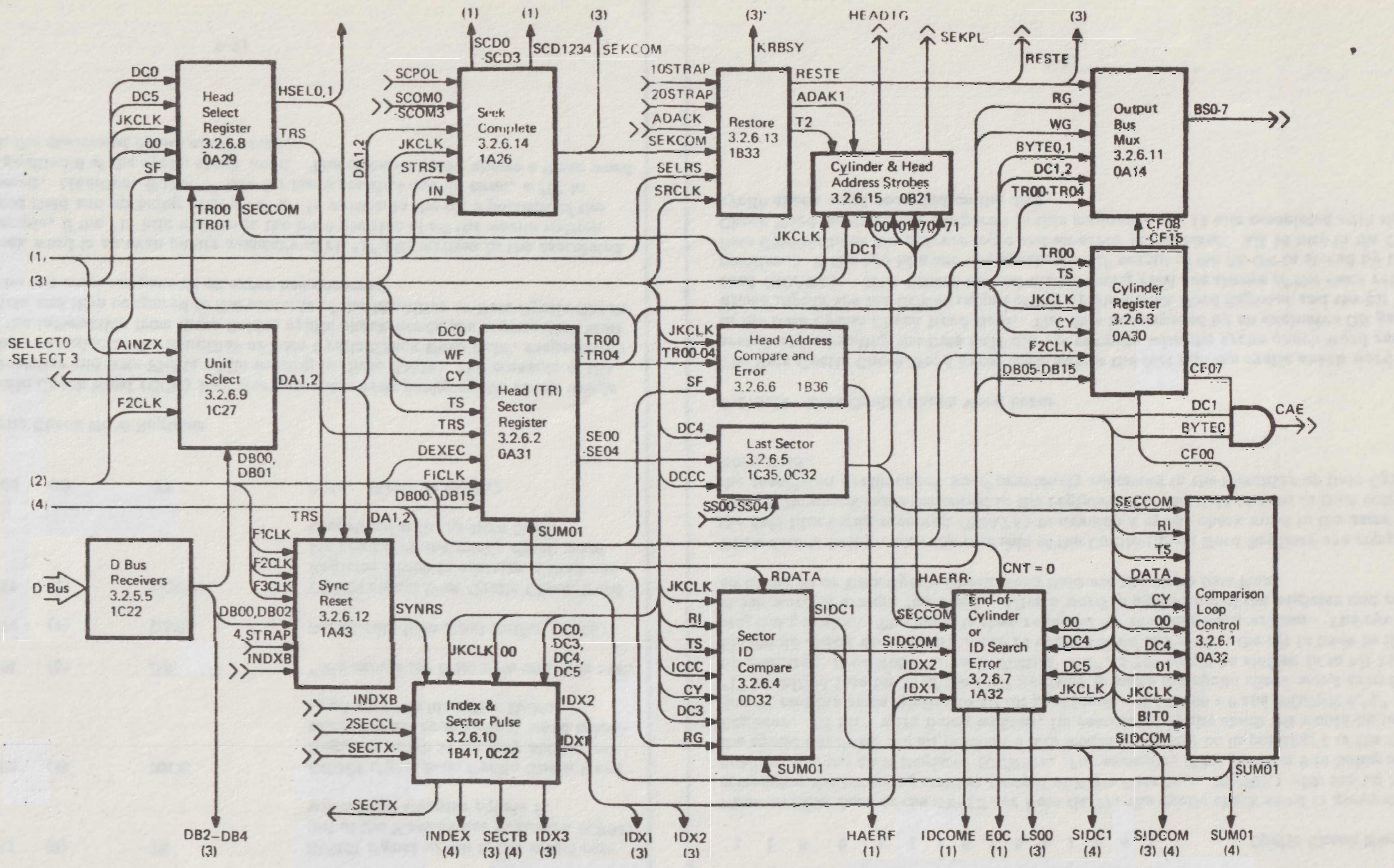
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bit Position
1	0	0	1	1	0	1	0	1	0	0	0	1	1	0	1	Word 1
0	0	1	1	0	1	1	0	1	1	0	0	1	0	1	0	Word 2
0	1	1	0	0	0	1	0	1	1	1	1	0	1	0	0	Word 3
1	1	0	0	1	1	1	0	1	0	1	1	0	0	1	1	Cyclic Check Word

When writing (and in the CY-TS, or Data field), the cyclic check word is generated by comparing the bit being written (output of Write Data Mux, WDMUX) with the bit in position 0 of the CCW Register (CCW00). For example, if bit position 0 is being written, the cyclic check bit for all position 0 bits would presently be in position 0 of the CCW Register. (If bit 1 were being written, its associated cyclic check bit would be in position 0, and the same applies to all bit positions). If CCW00 = 0 and WDMUX = "1" , a "1" is shifted into bit 15 of the CCW Register to make the cyclic check word even for that bit position. If CCW00 = "1" and WDMUX = "1", a "0" would be shifted in to bit 15 to keep the cyclic check word even. After 16 comparisons and shifts, the bit is back in its original position. The cycle is then repeated for the next word written. The cyclic check word is always "current". After a word is shifted out of the register and recorded in the ID or Data Cyclic Check Word field via the Write Data Mux.

When data is being read, the contents of the Cyclic Check Word Register are compared to the data bits being received (RDATA) to develop a cyclic check word in the same manner. The cyclic check word contained in the register after the field is read is then compared to the associated cyclic check word previously recorded in the Identifier or Data Cyclic Check Word field.

3.2.5.11 Data Cyclic Check Word Error

The Data Cyclic Check Word Error logic stores the fact that the cyclic check word regenerated while reading the Data field did not compare with the cyclic check word recorded in the Data Cyclic Check Word field. The data is compared by an exclusive OR gate whose inputs are the CCW00 output of the Cyclic Check Word Register and the bit being read (RDATA). (The CCW00 bit and the bit being read are always of the same relative position.) If the two bits are not equal, the "1" output of the EX OR is stored by the Data Cyclic Check Word Error logic and an error is indicated. All 16 bits in the Cyclic Check Word Register are compared in this manner to the 16 bits associated with the cyclic check word recorded on the disk.


Head Select Register 3.2.6.8 0A29
DC0
DC5
JKCLK
00
SF
HSEL0,1
TRS
TR00 TR01
SECCOM
DA1,2
(1)
(1)
(3)
SCD0 SCD3
SCD1234
SEKCOM
SCPOL
SCOM0 -SCOM3
Seek Complete 3.2.6.14 1A26
JKCLK
STRST
IN
10STRAP
20STRAP
ADACK
SEKCOM
SELRS
SRCLK
(3)
KRBSY
Restore 3.2.6.13 1B33
RESTE
ADAK1
T2
HEADIG
SEKPL
Cylinder & Head Address Strobes 3.2.6.15 0B21
00 01 70 71
JKCLK
DC1
(3)
RESTE
RG
WG
BYTE0,1
DC1,2
TR00-TR04
Output Bus Mux 3.2.6.11 0A14
BS0-7
CF08 -CF15
TR00
TS
JKCLK
CY
F2CLK
DB05-DB15
Cylinder Register 3.2.6.3 0A30
CF07
DC1
BYTE0
CAE
CF00
(1,
(3)
SELECT0 -SELECT 3
AINZX
F2CLK
Unit Select 3.2.6.9 1C27
DA1,2
DB00, DB01
DC0
WF
CY
TS
TRS
DEXEC
F1CLK
DB00-DB15
Head (TR) Sector Register 3.2.6.2 0A31
TR00 -TR04
SE00 -SE04
SUM01
JKCLK
TR00-04
SF
Head Address Compare and Error 3.2.6.6 1B36
DC4
DCCC
Last Sector 3.2.6.5 1C35, 0C32
SS00-SS04
(2)
(4)
D Bus
D Bus Receivers 3.2.5.5 1C22
DB00,DB02
4 STRAP
INDXB
TRS
DA1,2
F1CLK
F2CLK
F3CLK
Sync Reset 3.2.6.12 1A43
SYNRS
JKCLK
00
DC0, DC3, DC4, DC5
INDXB
2SECCL
SECTX
Index & Sector Pulse 3.2.6.10 1B41, 0C22
IDX2
IDX1
SECTX
DB2–DB4 (3)
INDEX (4)
SECTB (3) (4)
IDX3 (3)
IDX1 (3)
IDX2 (3)
RDATA
JKCLK
RI
TS
ICCC
CY
DC3
RG
Sector ID Compare 3.2.6.4 0D32
SIDC1
SUM01
HAERR
CNT = 0
SECCOM
SIDCOM
IDX2
IDX1
End-of-Cylinder or ID Search Error 3.2.6.7 1A32
00
DC4
DC5
JKCLK
SECCOM
RI
TS
DATA
CY
00
DC4
01
JKCLK
BIT0
SIDCOM
Comparison Loop Control 3.2.6.1 0A32
SUM01
HAERR (1)
IDCOME (1)
EOC (1)
LS00 (3)
SIDC1 (4)
SIDCOM (3) (4)
SUM01 (4)

Notes:
1. >> To or from disk drive.
2. > Jumper connections.
3. Numbers contained in boxes refer to paragraph and logic location.
4. Numbers in parenthesis identify a logic block in figure 3-1 as the source or destination of the indicated signal(s). Figures showing logic within each block are as follows:
   - Block 1, Processor Interface: figure 3-2, page 3-3
   - Block 2, DMA Control: figure 3-3, page 3-7
   - Block 3, Control Function: figure 3-5, page 3-15
   - Block 4, Read/Write Function: figure 3-6, page 3-24
   - Block 5, Disc Control and Interface: figure 3-7, page 3-30

Figure 3-7. Disk Control and Interface Function (5)

3.2.5.12 Identifier Cyclic Check Word Error

The Identifier Cyclic Check Word Error logic stores the fact that the cyclic check word regenerated while reading the Identifier field did not compare with the cyclic check word recorded in the Identifier Cyclic Check Word field. The data is compared when there has been a successful ID compare (SIDC1) and is executed in the same manner as for the Data Cyclic Check Word Error logic.

3.2.5.13 Read Gate

The Read Gate logic enables the Read Data and Read Clock lines in the selected disk drive at the appropriate times during Read or Write operations. It is also used in the Control function and elsewhere in the Read/Write function.

3.2.5.14 Write Gate

The Write Gate logic enables the Write (WRGT) and Erase (ERGT) currents in the addressed head of the selected disk drive at the appropriate times during Write Data or Write Format operations.

3.2.6 Disk Control and Interface Function (Figure 3-7)

3.2.6.1 Comparison Loop Control

The Comparison Loop Control output is used for updating the Head Sector Register as the Cylinder and Head Sector Registers are being rotated in unison during CY and TS time (when Field Counter equal 2 and 3). Its output, SUM01, is shifted into the MSB position of the Head Sector Register. After 32 shifts, all bits of the Cylinder and Head Sector Registers are back in their original positions. SUM01 is also applied to the Write Data Mux for recording the Cylinder-Head Sector address during a Write Format operation, and to the Sector ID Comparator to identify the proper sector(s) for processing.

3.2.6.2 Head Sector Register

The sector section of the Head Sector Register contains the address of the sector to be processed, in positions 00 thru 04 (SE00-04). After finding the starting sector (through use of the Sector ID Comparator) the Sector address is updated as each sector is processed (only if multi-sector operation is performed). The parallel output of the sector section

(SE00-04 only) is applied to the Last Sector Comparator to indicate when the maximum numbered sector is being processed.

The head section contains the address of the head which is enabled at the selected disk drive, in positions 00 thru 04. (TR00-04). The starting Head and Sector address is loaded from Word 1 of the Disk Control block. The Head address is updated after the maximum numbered sector on a particular track is processed (only if multi-head operation is performed). The low-order two bits of the head section (TR00 and TR01) are applied to the Head Select Register which stores the Head address for head selection at the selected disk drive (for disks containing a maximum of four heads only). The full parallel output of the head section (TR00 thru TR04) is applied to the Head Address Comparator to indicate when the maximum numbered head is being used, or for Head address error detection.

The Head Sector Register also contains flag bits in position 05 thru 07 of the Head section. Besides the Head Sector address, these flag bits must compare to whatever was written (in the corresponding positions) while recording the Head address in the ID field during disk formatting. If they do not compare, a sector compare will not be obtained.

3.2.6.3 Cylinder Register

The Cylinder Register contains the address of the cylinder being processed, as input from Word 2 of the Disk Control block. The Cylinder address is not updated as is the Head Sector address, for only one cylinder can be accessed with any one operation. The contents of the Cylinder Register are compared along with the Head Sector address for sector identification. The Cylinder Register contains two flag bits. These are located in positions 05 and 06. As with the flag bits in the Head Sector register, these bits must compare with the recorded data in the corresponding bit positions to obtain an ID compare. Register output signals CF08 thru CF15 are applied to the Output Bus Mux. CF07 is used to generate CAE if a 406 or 408 cylinder drive is being used. CF00 is used as the input to the Comparison Loop Control (Paragraph 3.2.6.1).

3.2.6.4 Sector ID Comparator

The Sector ID Comparator compares the contents one bit at a time of the Cylinder, and Head Sector Register to the Cylinder and Head Sector addresses recorded in the Identifier field of the sector presently under the enabled head. If the two compare, the designated sector has been found. If they do not compare, the Identifier of subsequent sectors will be compared until the designated sector is found, or an ID Search error (IDCOME) occurs (sector not found after searching all sectors of a particular track).

3.2.6.5 Last Sector

The Last Sector logic compares the contents of the sector section of the Head Sector Register (SE00 thru SE04 only) to the maximum numbered sector as designated by rear-edge connector (J11 on 531 board) strapping. When the two compare, the maximum numbered sector is being processed. Upon completion of this sector, the output of the logic (SECCOM) causes updating of the Head Select Register (TRS) and the resetting of the sector section of the Head Sector Register to 0. This is to allow the operation to continue at Sector 0 of the track associated with the next higher numbered head, if the word count has not been decremented to zero. The logic also enables detection of an End-of-Cylinder error.

3.2.6.6 Head Address Comparator and Error

The Head Address Comparator compares the contents of the head section (TR00-TR04) of the Head Sector Register to the maximum numbered head as designated by rear edge connector (J11 on 531 board) strapping when 4, 10, or 20 heads are used. (If no strapping is done, 2 heads are assumed.) If the two compare, the maximum numbered head is being used. The output of the Head Address Comparator (HAERR) is used for indicating an End-of-Cylinder error (EOC) if the maximum numbered sector has been completed, and the DMA word count has not been decremented to zero. HAERR combines with SECCOM (sector complete) and CNT = 0 (DMA word count equals zero) to clear the Disk Control Counter.

The Head Address Comparator also compares the contents of the Head Register for a specified head number greater than the maximum numbered head. This is done just after all four words of the Disk Control block have been extracted from Memory (SF signal true). If the specified head is greater, a Head Address error (HAERR) is indicated and a flip-flop is set (HAERF) which may be interrogated by Status input.

3.2.6.7 End-of-Cylinder and ID Search Error

The End-of-Cylinder and ID Search Error logic will indicate an End-of-Cylinder error if the maximum numbered head is being used, the maximum numbered sector is complete, and the DMA word count has not yet been decremented to zero (LS00). An ID Search error (IDCOME) will result if an ID compare did not occur during at least one revolution of the disk. These indications are stored and can be interrogated by Status input.

3.2.6.8 Head Select Register

The Head Select Register is comprised of two flip-flops which accept inputs from the Head Sector Register to store the address of the specified head for output to the selected disk

drive. It is only used for drives containing a maximum of four heads (numbered 0 thr 3). The outputs from the register are used by the selected disk drive to enable the sp fied head. If more than four heads are used, the outputs from the head section of the Sector Register (TR00-TR04) are transferred directly to the selected disk drive via th Output Bus Multiplexer.

3.2.6.9 Unit Select

The Unit Select logic is essentially comprised of two flip-flops which store the addres the specified disk drive. The unit address is contained in bits 0 and 1 of Word 2 of th Disk Control block. When Word 2 is extracted from Memory, the unit address is clock (F2CLK) directly into the two flip-flops for storage. The logic then outputs a signal (SELECT 0 - SELECT 3) enabling the selected disk drive. The logic also outputs cont signals (DA1 and DA2) within the disk controller to indicate the selected unit to vario functions (Multiplexers, etc.).

3.2.6.10 Index and Sector Pulse

The Index and Sector Pulse logic develops an Index "pulse" to indicate the start of Se 0. The logic accepts raw Index "marks" from the selected disk drive, which occur at beginning of the maximum numbered sector. It then develops the Index pulse from th Index mark upon occurrence of the next Sector pulse. The Sector pulses (SECT B) w be the same frequency as the raw sector marks or half the frequency if the Divide-By logic is implemented by rear edge connector J11 strapping.

The index pulses are stored to indicate an error if two pulses are developed without t occurrence of an ID compare. This indicates at least one full revolution of the disk oc ed without finding the specified sector. This error (IDCOME) causes termination of t operation. (Refer to paragraphs 3.2.3.7 and 3.2.6.7.)

3.2.6.11 Output Bus Mux

The Output Bus Mux is mainly used to output the most significant eight bits of the Cylinder Register (CF-15-CF08) to the selected disk drive. If the disk drive(s) cont more than four heads, it is also used to output the head address (TR04-TR00). Read Write gate, Erase gate, and Restore (RESTE) signals can also be output via the Outpu Mux.

3.2.6.12 Sync Reset

The Sync Reset logic resynchronizes the controller to a new source of Index and Sector marks. This occurs when a different disk drive is being selected from the one used previously, or when the head being selected is associated with a different disk platter (4-head drives only). The Sync Reset logic output resets the Index and Sector Pulse logic circuits to prevent any Index or Sector pulses until an Index mark from the new source is received.

3.2.6.13 Restore

The Restore logic causes the heads at the selected disk drive to be restored to Cylinder 0. It is enabled directly from the Processor by a Select command using a function code of 4 (SELRS). The logic is normally implemented after a seek error has occurred at the selected disk drive.

3.2.6.14 Seek Complete

The Seek Complete logic buffers the Seek Complete signals from the on-line disk drives, corrects their polarity for proper integration with controller logic, and outputs the one associated with the selected unit. Its output (SEKCOM) causes the Disk Control Counter to be incremented to DC3, or the Restore logic to be reset.

The status section of the Seek Complete logic is comprised of four seperate status enable and store circuits, each associated with one of the four possible on-line disk drives. Storage of the seek complete signal is enabled when the cylinder address is sent to the selected disk drive. The received seek complete signal is then stored. The stored signal can be made to cause an interrupt, and is available to the Processor via Sense or Status input.

3.3 WRITE DATA OPERATION

As many as four Processor I/O commands are required to write data at an on-line disk drive. These are:

1. Sense Controller Not Busy
2. Initiate Write Data Function
3. Sense Controller Not Busy
4. Input Status

Each of these commands are described below. The specific command mentioned (SEN, OTA, INA) may be one of several which could be used. All, however, would operate in essentially the same manner within the disk controller.

Assume the disk drive to be used is a Diablo containing four heads with 12 sectors per track. It is running at 2400 RPM and 256 words per sector have been assigned by rear-edge connector J11 strapping. The following parameters will be specified when the Write Data function is initiated:

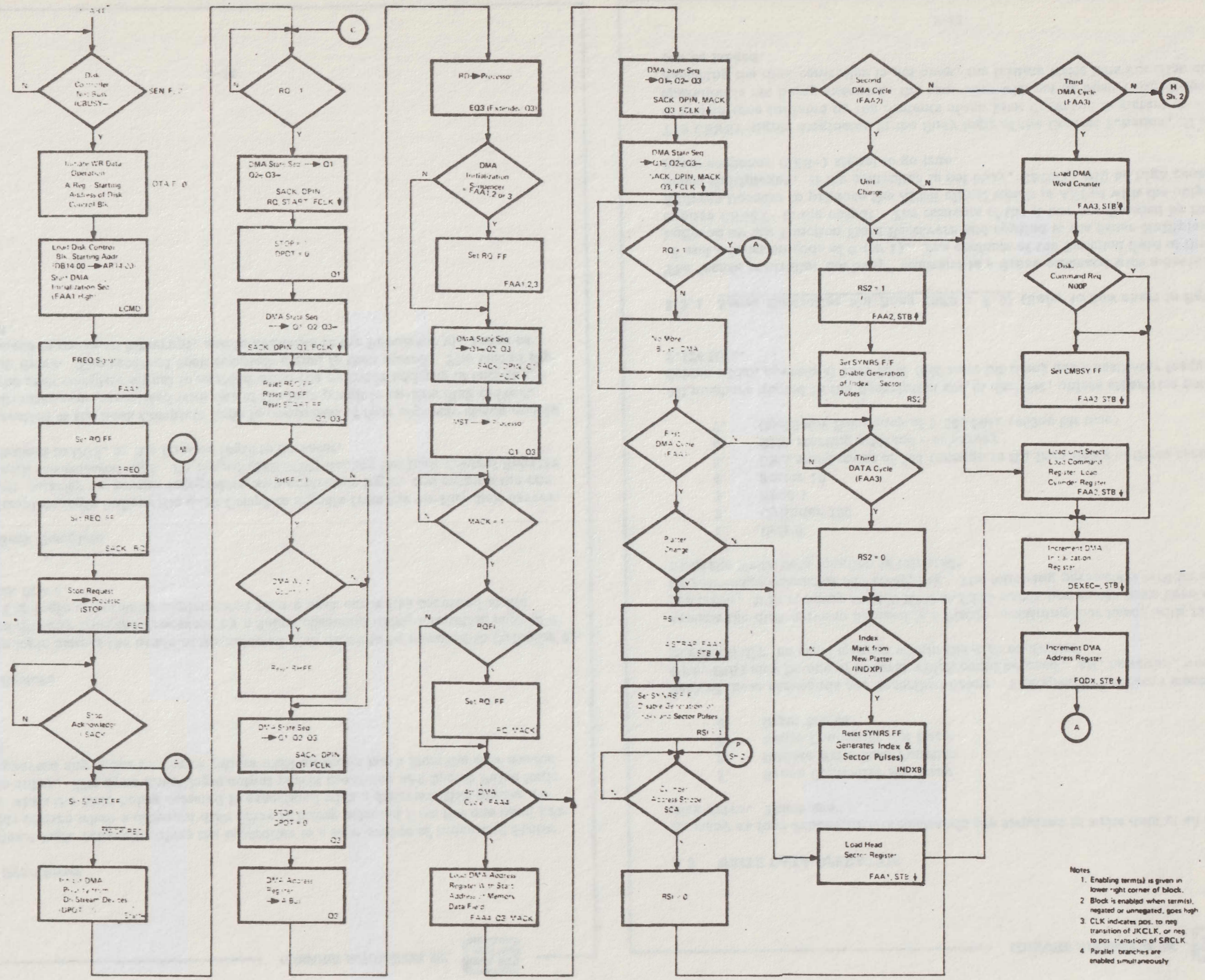
1. Unit 0
2. Cylinder 100
3. Head 1
4. Sector 10
5. DMA word count of 768 (enough to fill Data fields of three sectors)
6. DMA starting address - arbitrary
7. Oscillator frequency of 5.000 MHz (400ns bit time)

All numbers quoted in the description are in decimal, unless otherwise noted. Disk drives which operate at 1500 RPM (640 nsec bit time) use a oscillator frequency of 3.124 MHz.

3.3.1 Sense Controller Not Busy (SEN : F,0) (Refer to flow chart in figure 3-8)

The "sense controller not busy" command is a Sense command with a device address of :F and a function code of 0 (or 1). The contents of the Function field of the A bus are buffered by the Function Field Receivers and applied to the Sense Multiplexer which applies CBUSY- to the output. The contents of the A bus are decoded by the Device Address Decoder to produce the ADDR signal which is ANDed with the output of the Sense Multiplexer. If the controller is not busy, CBUSY- will be high causing the sense response (SER-) signal to go true.

The CBUSY signal originates in the Busy logic of the Control Function. If a "disk" command (one initiated by the contents of the Disk Command Register) or a Restore operation is not being executed, the controller will not be busy (CBUSY low). Assuming the disk controller is not busy, the Initiate Write Data Function command can be issued.


A-11
Disk Controller Not Busy (CBUSY–)
N
Y
SEN F, 0
Initiate WR Data Operation
A Reg – Starting Address of Disk Control Blk
OTA F, 0
Load Disk Control Blk. Starting Addr (DB14-00 → AR14-00)
Start DMA Initialization Seq (FAA1 High)
LCMD
FREQ Signal
FAA1
Set RQ FF
FREQ
M
Set REC FF
SACK, RQ
Stop Request → Processor (STOP)
REC
Stop Acknowledge (SACK)
A
Set START FF
MACK, REC
Inhibit DMA Priority from Dn Stream Devices (DPOT = 0)
Start
C
RQ = 1
DMA State Seq → Q1 Q2– Q3–
SACK, DPIN RQ, START, FCLK
STOP = 1
DPOT = 0
Q1
DMA State Seq → Q1 Q2 Q3–
SACK, DPIN, Q1, FCLK
Reset REC FF
Reset RQ FF
Reset START FF
Q1, Q3–
RHFF = 1
DMA Word Count = 1
Reset RHFF
DMA State Seq → Q1 Q2 Q3
SACK, DPIN Q1, FCLK
STOP = 1
DPOT = 0
Q3
DMA Address Register → A Bus
Q3
RD → Processor
EQ3 (Extended Q3)
DMA Initialization Sequencer = FAA1, 2 or 3
Set RQ FF
FAA1, 2, 3
DMA State Seq → Q1– Q2 Q3
SACK, DPIN, Q1, FCLK
MST → Processor
Q1, Q3
MACK = 1
RQFI
Set RQ FF
RQ, MACK
4th DMA Cycle (FAA4)
Load DMA Address Register With Start Address of Memory Data Field
FAA4, Q3, MACK
DMA State Seq → Q1– Q2– Q3
SACK, DPIN, MACK Q3, FCLK
DMA State Seq → Q1– Q2– Q3–
SACK, DPIN, MACK Q3, FCLK
RQ = 1
A
No More Burst DMA
First DMA Cycle (FAA1)
Platter Change
RS1 = 1
ASTRAP, FAA1 STB
Set SYNRS F/F Disable Generation of Index and Sector Pulses
RS1 = 1
P Sh 2
Cylinder Address Strobe SCA
RS1 = 0
Second DMA Cycle (FAA2)
Unit Change
RS2 = 1
FAA2, STB
Set SYNRS F/F Disable Generation of Index Sector Pulses
RS2
Third DATA Cycle (FAA3)
RS2 = 0
Index Mark from New Platter (INDXP)
Reset SYNRS FF Generates Index & Sector Pulses)
INDXB
Load Head Sector Register
FAA1, STB
Third DMA Cycle (FAA3)
H Sh. 2
Load DMA Word Counter
FAA3, STB
Disk Command Req N00P
Set CMBSY FF
FAA3, STB
Load Unit Select Load Command Register Load Cylinder Register
FAA2, STB
Increment DMA Initialization Register
DEXEC–, STB
Increment DMA Address Register
FQDX, STB
A

Notes
1. Enabling term(s) is given in lower right corner of block.
2. Block is enabled when term(s), negated or unnegated, goes high
3. CLK indicates pos. to neg transition of JKCLK, or neg to pos transition of SRCLK
4. Parallel branches are enabled simultaneously

Figure 3-8. Write Data Flow Chart Sheet 1

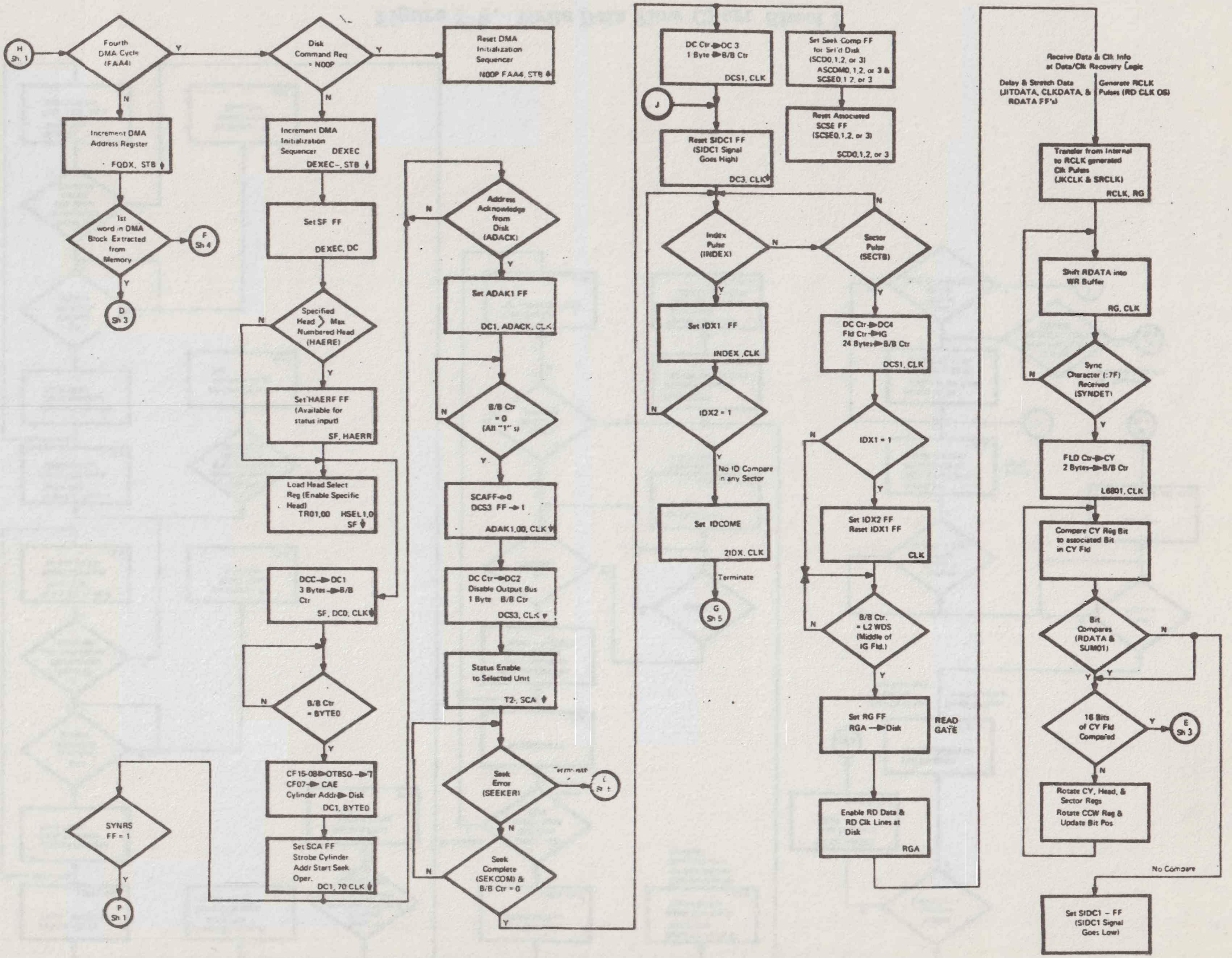

H Sh. 1
Fourth DMA Cycle (FAA4)
Y
N
Increment DMA Address Register
FQDX, STB
1st word in DMA Block Extracted from Memory
F Sh 4
Y
D Sh 3
Disk Command Req = N00P
Y
N
Increment DMA Initialization Sequencer DEXEC
DEXEC–, STB
Set SF FF
DEXEC, DC
Specified Head > Max Numbered Head (HAERE)
N
Y
Set HAERF FF (Available for status input)
SF, HAERR
Load Head Select Reg (Enable Specific Head)
TR01,00 HSEL1,0
SF
DCC→DC1
3 Bytes→B/B Ctr
SF, DC0, CLK
B/B Ctr = BYTE0
N
Y
CF15-08→OTBS0-→7
CF07→CAE
Cylinder Addr→Disk
DC1, BYTE0
Set SCA FF
Strobe Cylinder Addr Start Seek Oper.
DC1, 70 CLK
SYNRS FF = 1
Y
P Sh 1
Reset DMA Initialization Sequencer
N00P FAA4, STB
Address Acknowledge from Disk (ADACK)
N
Y
Set ADAK1 FF
DC1, ADACK, CLK
B/B Ctr = 0 (All "1" s)
N
Y
SCAFF→0
DCS3 FF→1
ADAK1,00, CLK
DC Ctr→DC2
Disable Output Bus
1 Byte B/B Ctr
DCS3, CLK
Status Enable to Selected Unit
T2-, SCA
Seek Error (SEEKER)
Terminate
N
Seek Complete (SEKCOM) & B/B Ctr = 0
N
Y
DC Ctr→DC 3
1 Byte→B/B Ctr
DCS1, CLK
J
Reset SIDC1 FF (SIDC1 Signal Goes High)
DC3, CLK
Set Seek Comp FF for Sel'd Disk (SCD0,1,2, or 3)
ASCOM0,1,2, or 3 &
SCSE0,1,2, or 3
Reset Associated SCSE FF (SCSE0,1,2, or 3)
SCD0,1,2, or 3
Index Pulse (INDEX)
N
Y
Set IDX1 FF
INDEX ,CLK
IDX2 = 1
N
Y
No ID Compare in any Sector
Set IDCOME
2IDX, CLK
Terminate
G Sh 5
Sector Pulse (SECTB)
N
Y
DC Ctr→DC4
Fld Ctr→IG
24 Bytes→B/B Ctr
DCS1, CLK
IDX1 = 1
N
Y
Set IDX2 FF
Reset IDX1 FF
CLK
B/B Ctr. = L2 WDS (Middle of IG Fld.)
N
Y
Set RG FF
RGA→Disk
READ GATE
Enable RD Data & RD Clk Lines at Disk
RGA
Receive Data & Clk Info at Data/Clk Recovery Logic
Delay & Stretch Data (JITDATA, CLKDATA, & RDATA FF's)
Generate RCLK Pulses (RD CLK OS)
Transfer from Internal to RCLK generated Clk Pulses (JKCLK & SRCLK)
RCLK, RG
Shift RDATA into WR Buffer
RG, CLK
Sync Character (:7F) Received (SYNDET)
N
Y
FLD Ctr→CY
2 Bytes→B/B Ctr
L6801, CLK
Compare CY Reg Bit to associated Bit in CY Fld
Bit Compares (RDATA & SUM01)
N
Y
Y
16 Bits of CY Fld Compared
Y
E Sh 3
N
Rotate CY, Head, & Sector Regs
Rotate CCW Reg & Update Bit Pos
No Compare
Set SIDC1 – FF (SIDC1 Signal Goes Low)

Figure 3-8. Write Data Flow Chart Sheet 2

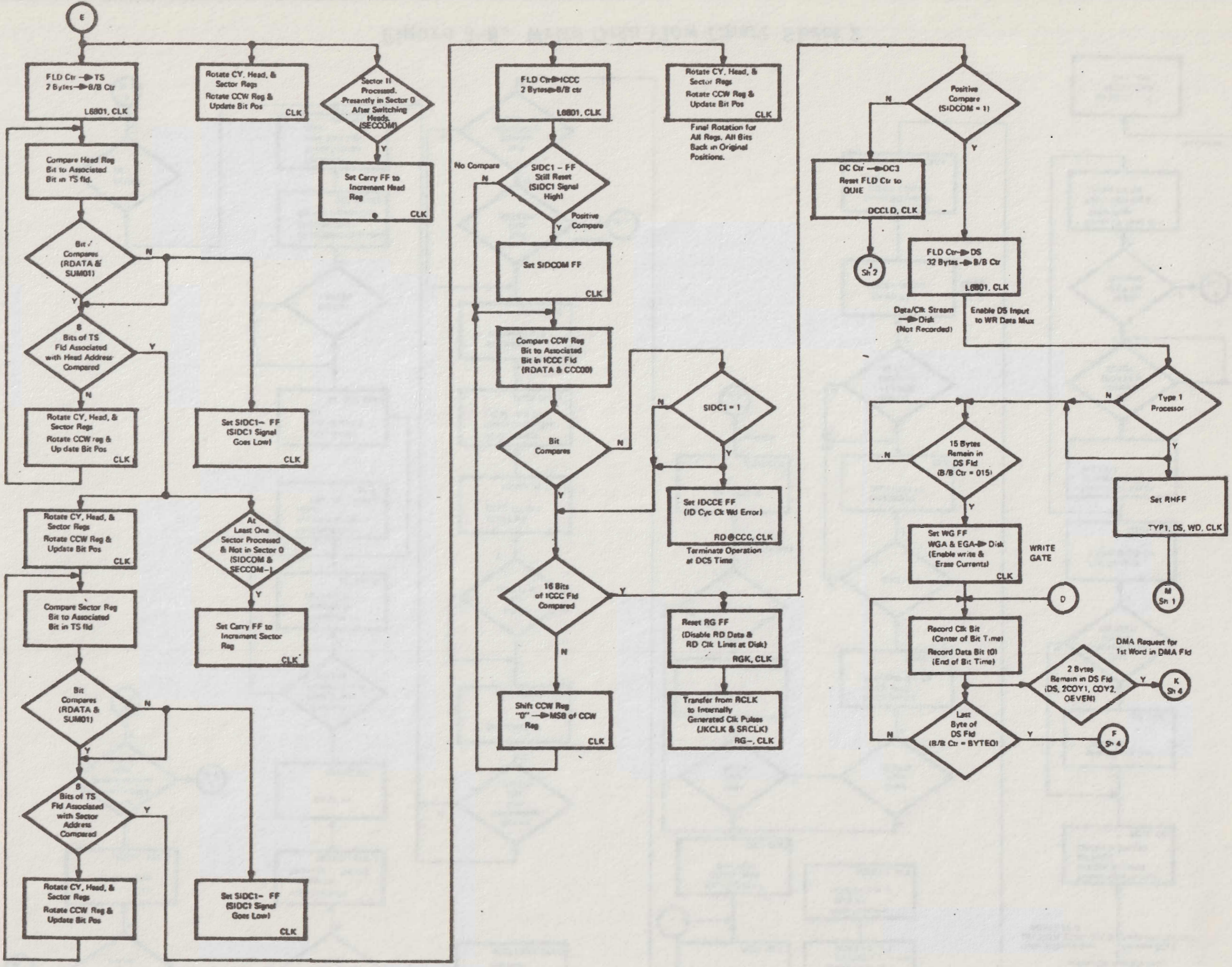

E
FLD Ctr → TS
2 Bytes → B/B Ctr
L6801, CLK
Compare Head Reg Bit to Associated Bit in TS fld.
Bit Compares (RDATA & SUM01)
N
Y
8 Bits of TS Fld Associated with Head Address Compared
Y
N
Rotate CY, Head, & Sector Regs
Rotate CCW reg & Up date Bit Pos
CLK
Set SIDC1– FF (SIDC1 Signal Goes Low)
CLK
Rotate CY, Head, & Sector Regs
Rotate CCW Reg & Update Bit Pos
CLK
Sector II Processed. Presently in Sector 0 After Switching Heads. (SECCOM)
Y
Set Carry FF to Increment Head Reg
CLK
Rotate CY, Head, & Sector Regs
Rotate CCW Reg & Update Bit Pos
CLK
At Least One Sector Processed & Not in Sector 0 (SIDCOM & SECCOM–)
Y
Set Carry FF to Increment Sector Reg
CLK
Compare Sector Reg Bit to Associated Bit in TS fld
Bit Compares (RDATA & SUM01)
N
Y
8 Bits of TS Fld Associated with Sector Address Compared
Y
Rotate CY, Head, & Sector Regs
Rotate CCW Reg & Update Bit Pos
Set SIDC1– FF (SIDC1 Signal Goes Low)
CLK
FLD Ctr → ICCC
2 Bytes → B/B ctr
L6801, CLK
No Compare
N
SIDC1 – FF Still Reset (SIDC1 Signal High)
Positive Compare
Y
Set SIDCOM FF
CLK
Compare CCW Reg Bit to Associated Bit in ICCC Fld (RDATA & CCC00)
Bit Compares
N
Y
SIDC1 = 1
N
Y
Set IDCCE FF (ID Cyc Ck Wd Error)
RD⊕CCC, CLK
Terminate Operation at DCS Time
16 Bits of ICCC Fld Compared
Y
N
Shift CCW Reg "0" → MSB of CCW Reg
CLK
Rotate CY, Head, & Sector Regs
Rotate CCW Reg & Update Bit Pos
CLK
Final Rotation for All Regs. All Bits Back in Original Positions.
Reset RG FF (Disable RD Data & RD Clk Lines at Disk)
RGK, CLK
Transfer from RCLK to Internally Generated Clk Pulses (JKCLK & SRCLK)
RG–, CLK
Positive Compare (SIDCOM = 1)
N
Y
DC Ctr → DC3
Reset FLD Ctr to QUIE
DCCLD, CLK
J
Sh 2
FLD Ctr → DS
32 Bytes → B/B Ctr
L6801, CLK
Data/Clk Stream → Disk (Not Recorded)
Enable DS Input to WR Data Mux
Type 1 Processor
N
Y
Set RHFF
TYP1, DS, WD, CLK
M
Sh 1
15 Bytes Remain in DS Fld (B/B Ctr = 015)
N
Y
Set WG FF
WGA & EGA → Disk
(Enable write & Erase Currents)
CLK
WRITE GATE
D
Record Clk Bit (Center of Bit Time)
Record Data Bit (0) (End of Bit Time)
DMA Request for 1st Word in DMA Fld
2 Bytes Remain in DS Fld (DS, 2COY1, COY2, OEVEN)
Y
K
Sh 4
Last Byte of DS Fld (B/B Ctr = BYTEO)
N
Y
F
Sh 4

Figure 3-8. Write Data Flow Chart Sheet 3

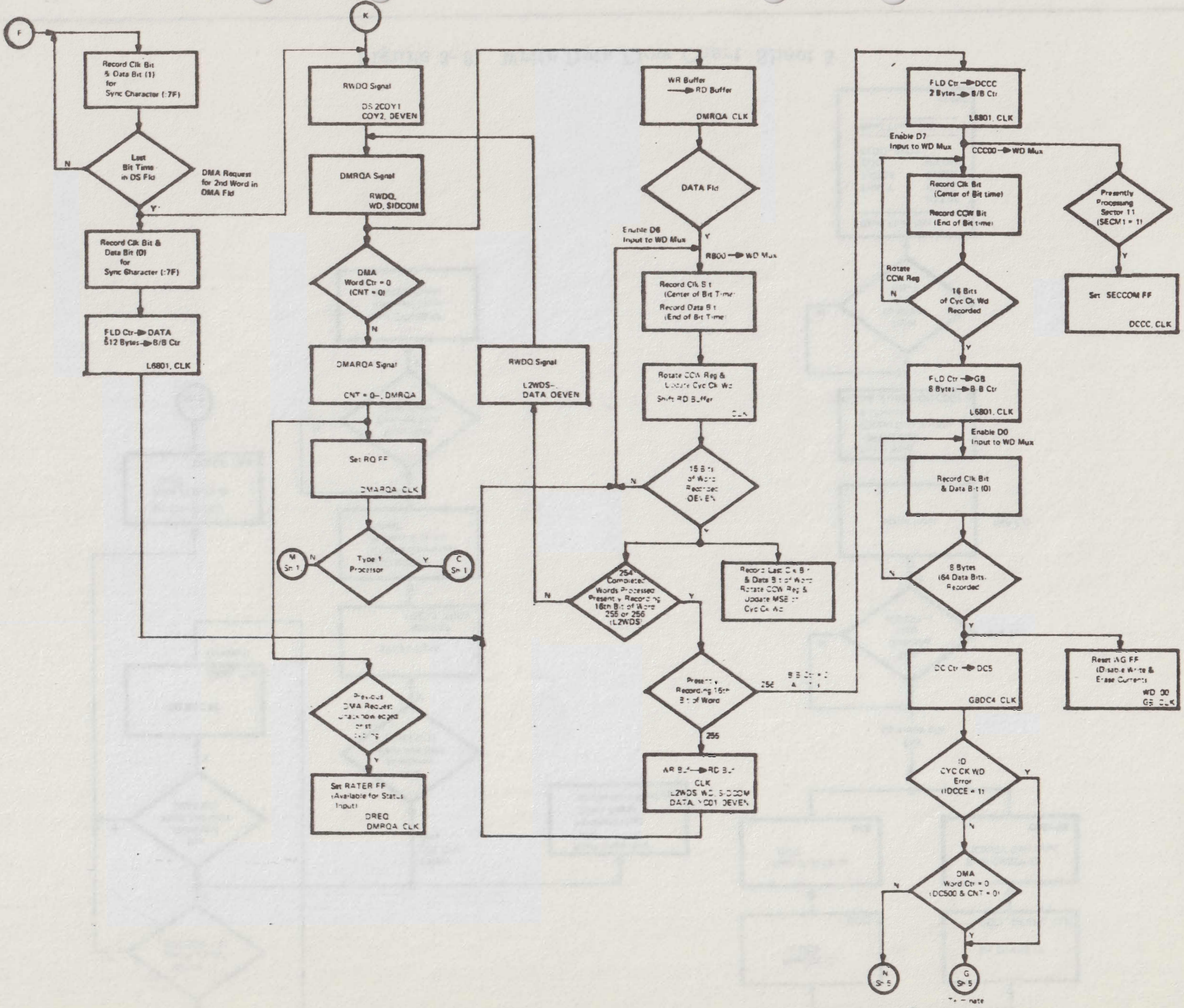

F
Record Clk Bit
& Data Bit (1)
for
Sync Character (:7F)
Last
Bit Time
in DS Fld
N
Y
DMA Request
for 2nd Word in
DMA Fld
Record Clk Bit &
Data Bit (0)
for
Sync Character (:7F)
FLD Ctr → DATA
512 Bytes → B/B Ctr
L6801, CLK
K
RWDO Signal
DS 2COY1
COY2, DEVEN
DMRQA Signal
RWDQ,
WD, SIDCOM
DMA
Word Ctr = 0
(CNT = 0)
N
DMARQA Signal
CNT = 0–, DMRQA
Set RQ FF
DMARQA CLK
M
Sh 1
N
Type 1
Processor
Y
C
Sh 1
Previous
DMA Request
Unacknowledged
Y
Set RATER FF
(Available for Status
Input)
DREQ
DMRQA CLK
RWDQ Signal
L2WDS–,
DATA OEVEN
N
254
Completed
Words Processed
Presently Recording
16th Bit of Word
255 or 256
(L2WDS)
Y
WR Buffer
→ RD Buffer
DMRQA CLK
DATA Fld
Y
Enable D6
Input to WD Mux
RB00 → WD Mux
Record Clk Bit
(Center of Bit Time)
Record Data Bit
(End of Bit Time)
Rotate CCW Reg &
Update Cyc Ck Wd
Shift RD Buffer
CLK
15 Bits
of Word
Recorded
OEVEN
N
Y
Record Last Clk Bit
& Data Bit of Word
Rotate CCW Reg &
Update MSB of
Cyc Ck Wd
Presently
Recording 16th
Bit of Word
256
B B Ctr = 0
255
WR Buf → RD Buf
CLK
L2WDS WD, SIDCOM
DATA, YC01 DEVEN
FLD Ctr → DCCC
2 Bytes → B/B Ctr
L6801, CLK
Enable D7
Input to WD Mux
CCC00 → WD Mux
Record Clk Bit
(Center of Bit time)
Record CCW Bit
(End of Bit time)
Rotate
CCW Reg
N
16 Bits
of Cyc Ck Wd
Recorded
Y
Presently
Processing
Sector 11
(SECM1 = 1)
Y
Set SECCOM FF
DCCC, CLK
FLD Ctr → GB
8 Bytes → B/B Ctr
L6801, CLK
Enable D0
Input to WD Mux
Record Clk Bit
& Data Bit (0)
N
8 Bytes
(64 Data Bits)
Recorded
Y
DC Ctr → DC5
GBDC4 CLK
Reset WG FF
(Disable Write &
Erase Currents)
WD 00
GB CLK
ID
CYC CK WD
Error
(IDCCE = 1)
Y
N
DMA
Word Ctr = 0
(DC500 & CNT = 0)
N
Y
N
Sh 5
G
Sh 5
Terminate

Figure 3-8. Write Data Flow Chart Sheet 4

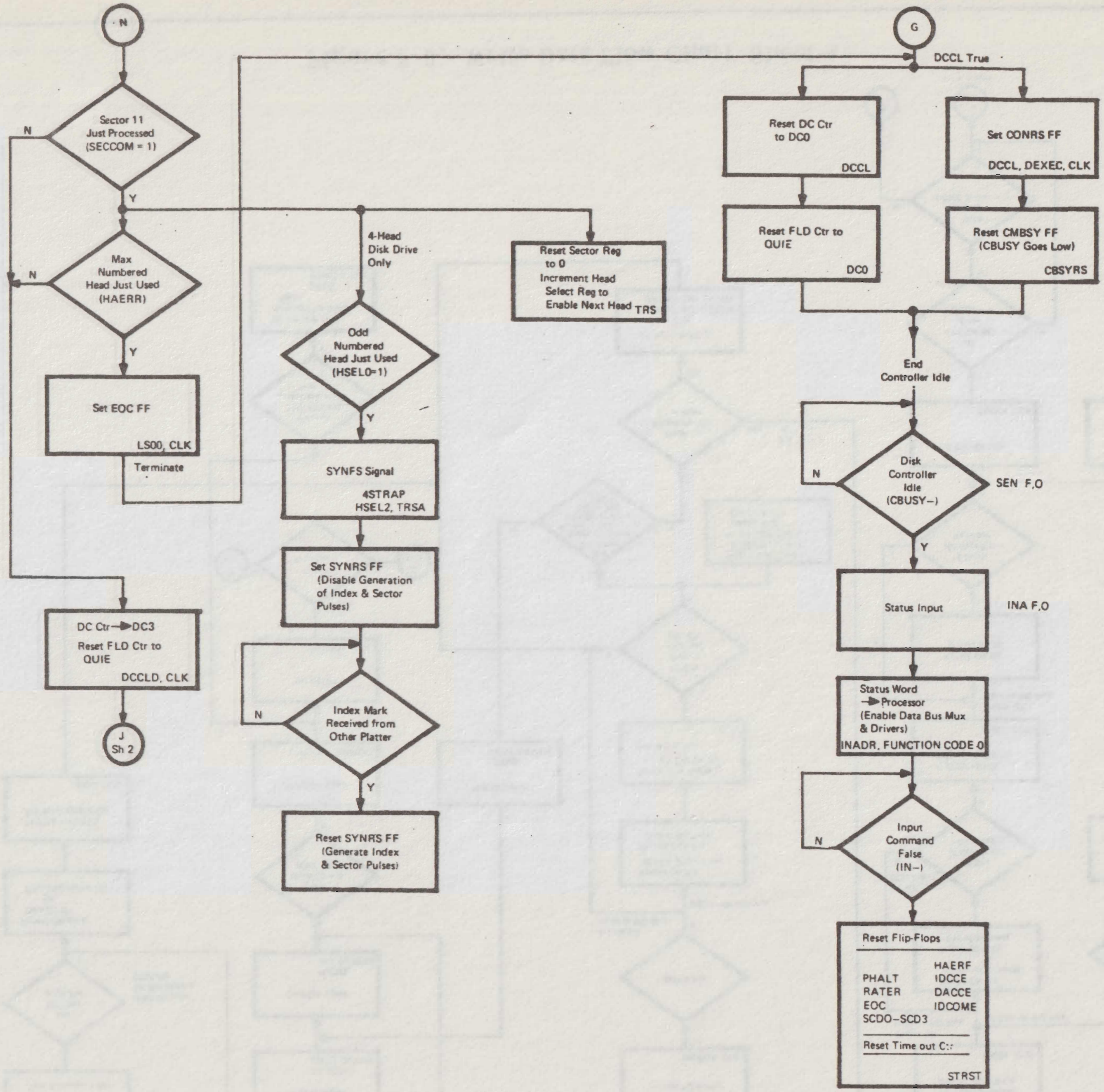

N
Sector 11
Just Processed
(SECCOM = 1)
N
Y
Max
Numbered
Head Just Used
(HAERR)
N
Y
Set EOC FF
LS00, CLK
Terminate
DC Ctr → DC3
Reset FLD Ctr to
QUIE
DCCLD, CLK
J
Sh 2
4-Head
Disk Drive
Only
Odd
Numbered
Head Just Used
(HSEL0=1)
Y
SYNFS Signal
4STRAP
HSEL2, TRSA
Set SYNRS FF
(Disable Generation
of Index & Sector
Pulses)
Index Mark
Received from
Other Platter
N
Y
Reset SYNRS FF
(Generate Index
& Sector Pulses)
Reset Sector Reg
to 0
Increment Head
Select Reg to
Enable Next Head
TRS
G
DCCL True
Reset DC Ctr
to DC0
DCCL
Reset FLD Ctr to
QUIE
DC0
Set CONRS FF
DCCL, DEXEC, CLK
Reset CMBSY FF
(CBUSY Goes Low)
CBSYRS
End
Controller Idle
Disk
Controller
Idle
(CBUSY–)
N
Y
SEN F,O
Status Input
INA F,O
Status Word
→ Processor
(Enable Data Bus Mux
& Drivers)
INADR, FUNCTION CODE 0
Input
Command
False
(IN–)
N
Reset Flip-Flops
PHALT
RATER
EOC
SCD0–SCD3
HAERF
IDCCE
DACCE
IDCOME
Reset Time out Ctr
STRST

Figure 3-8. Write Data Flow Chart Sheet 5

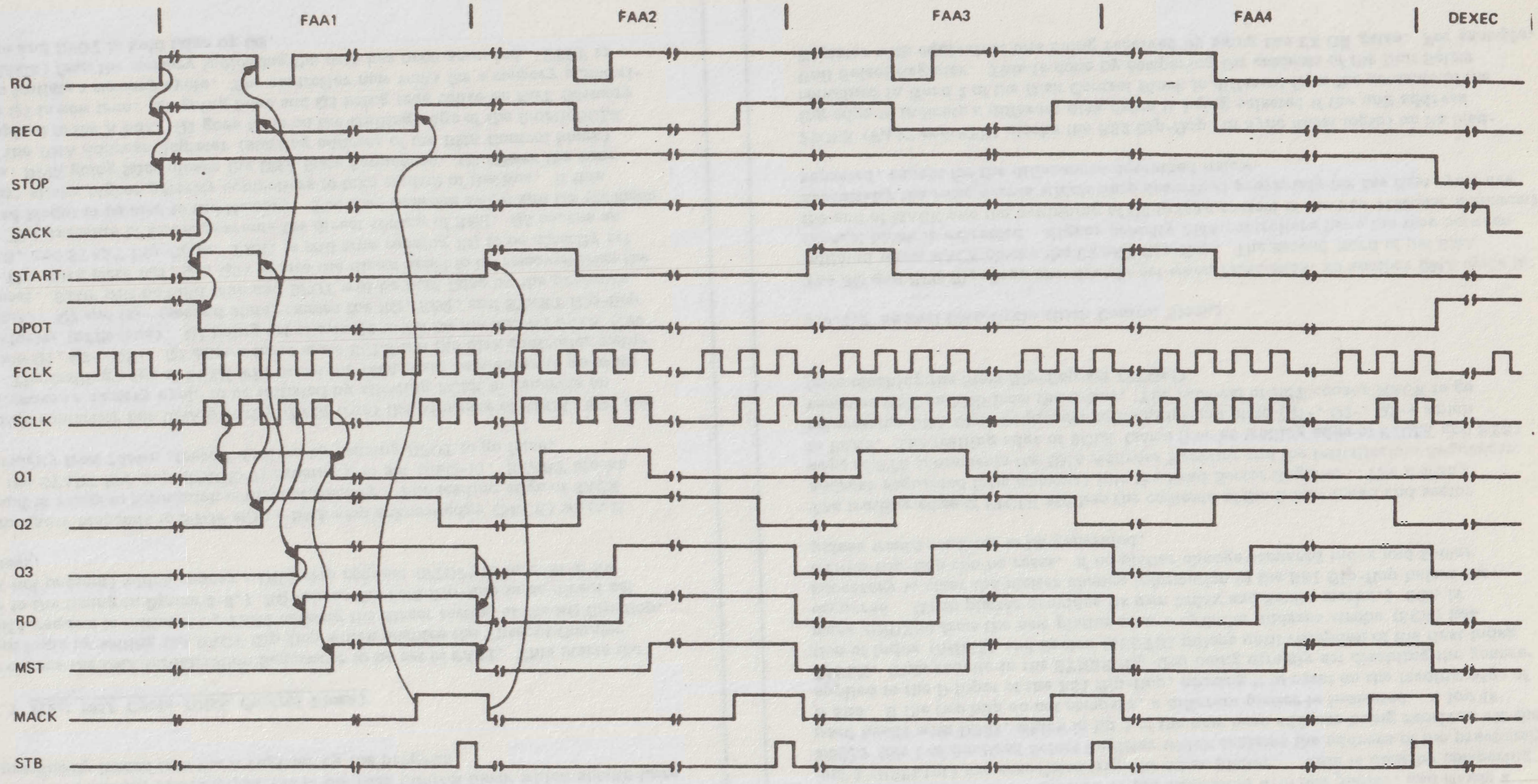

FAA1
FAA2
FAA3
FAA4
DEXEC
RQ
REQ
STOP
SACK
START
DPOT
FCLK
SCLK
Q1
Q2
Q3
RD
MST
MACK
STB

Figure 3-9. Disk Control Block Acquisition

3.3.2 Initiate Write Data Function (OTA :F,0) (Figure 3-9)

The "initiate write data function" command is an Output A register command with a device address of :F and a function code of 0. The device address is decoded by the Device Address Decoder which produces the ADDR signal. ADDR is applied to the I/O Command Decode logic where it is NANDed with CBUSY- (presently high) and OUT, which goes high during the Output command. The result is DOUT which is NANDed with PLSE (true for a nominal 200ns) and EMASK- to produce LCMD. LCMD causes the DMA Address Register to be parallel loaded with the D bus lines 0 thru 14. The D bus contains the starting address of the Disk Control block which should have been previously loaded into the A register by the program.

3.3.2.1 First DMA Cycle (Disk Control Block)

LCMD causes the DMA Initialization Sequencer to be set to FAA1. This starts the Timeout logic by setting the DACT flip-flop which enables the Timeout Counter. The DMA request is initiated by FAA1 causing the direct setting of the RQ flip-flop. (Refer to the timing in figure 3-9.) RQ causes the REQ flip-flop to be direct set (SACK not present) which causes a DMA stop request (STOP) to be sent to the Processor.

The Processor responds to STOP with a DMA stop acknowledge (SACK) when it stops and is ready to relinquish control of Memory. The leading edge of SACK clocks the START flip-flop (MACK=0) causing it to set (REQ=1). START blocks DMA priority from "down stream" devices by causing DPOT to go false.

If the disk controller has DMA priority (DPIN true) the presence of SACK, RQ, and START causes a memory cycle to be initiated by allowing FCLK to generate an SCLK. The trailing edge of SCLK will cause the DMA State Sequencer to go to its first state Q1, Q2-, Q3-. Q1 allows three more SCLK's if the disk controller maintains priority (DPIN true). Q1 being set allows Q2 to set on the second SCLK (100 nsec later). Q2 and Q3- (second state) causes the RQ, REQ, and START flip-flop to be reset. STOP will be held true and DPOT will be held false by the presence of Q1. The third state (Q1, Q2, Q3) causes the direct reset to be removed from the RQ, REQ, and START flip-flops. FAA1 is still true causing RQ to be directly set again. The presence of SACK prevents the direct setting of REQ. Q3 causes an RD (Read Mode) to be sent to the Memory. The time between SACK and Q3 (200nsec minimum) allows higher priority controllers to take control of the bus. If this happens, DPIN going false clears the DMA State Sequencer. Q3 allows the contents of the DMA Address Register (starting address of the DMA Control block) to be applied to the A bus. Q1 goes false on the trailing edge of the fourth SCLK because Q3 is now true. Q1 going false and Q3 being true cause an MST (Memory Start) to initiate a memory cycle. The controller now waits for a memory acknowledge (MACK) from the memory indicating the data has been accessed. STOP is held true and DPOT is held false by Q3.

The leading edge of MACK sets the REQ flip-flop (RQ is true) insuring "burst" mode operation. The presence of MACK and Q3 allows two more SCLK's, the first moves the DMA State Sequencer to the fifth state (Q1-, Q2-, Q3). The last SCLK of the first DMA cycle generates STB.

STB and FAA1 generate F1CLK which is used in the Sync Reset logic to clock RS1 true if four heads (2 disk platters) are being used in the disk drive(s), and the head being addressed is associated with a different platter from the one used previously. Heads 0 and 1 (HSEL1=0) are associated with one platter, and Heads 2 and 3 (HSEL1=1) are associated with the other platter. This is done by comparing HSEL2 (bit 1 of the Head Select Register which contains the address of the previously used head) with DB01, which is bit 1 of the new head address being received via the D bus. If the two bits do not compare, a different platter is indicated. A low is applied to the D input of the RS1 flip-flop, causing it to reset on the leading edge of F1CLK. This results in the SYNRS flip-flop being directly set disabling the generation of Index (INDEX) and Sector (SECTB) pulses until reception of the first Index mark (INDXB) from the new platter after a cylinder address strobe (SCA) has occurred. (Each platter provides its own Index and Sector marks.) SCA is necessary to clear the platter change information in the RS1 flip-flop before the SYNRS flip-flop can be reset. If no platter change occurred Index and Sector pulses would continue to be generated.

The trailing edge of F1CLK strobes the contents of the D bus (head and sector address requested from memory) into the Head Sector Register. The trailing edge of STB increments the DMA Address Register and the Intitalization Sequencer to FAA2. The trailing edge of SCLK (same time as trailing edge of F1CLK and STB) returns the DMA State Sequencer to its quiescent state (Q1-, Q2-, Q3-) which removes MST and RD from the C bus. The removal of MST causes MACK to go false clocking the Start flip-flop set (REQ=1).

3.3.2.2 Second DMA Cycle (Disk Control Block)

The RQ and REQ flip-flops are already set when FAA1 ends, so another DMA cycle is initiated when MACK clocks the START flip-flop. The second word of the DMA Control block is extracted. Higher priority DMA controllers have the time between the end of MACK and the beginning of Q3 to take control of the bus (200nsec minimum). Essentially the same events which were described previously for the first cycle are repeated, except for the differences described below.

F2CLK (FAA2 and STB) clocks the RS2 flip-flop (in Sync Reset logic) on its leading edge to indicate a different disk drive is being selected if the unit address contained in Word 2 of the Disk Control Block is different from the contents of the Unit Select Register. This is done by comparing the contents of the Unit Select Register with equivalent bits being received by using two EX OR gates. For example, if Unit 0 had been selected, and Unit 1 is to be selected, the DA1- input to one of the gates would be high, and the DB00 input to the same gate would also be high. The output would cause a high to be applied to the D input of the RS2 flip-flop. The flip-flop is then set on the leading edge of F2CLK which will disable generation of Index and Sector pulses as described previously in the first DMA cycle description. The RS2 flip-flop is cleared by F3CLK at the end of the third DMA cycle. Assuming the same unit is selected (Unit 0), no action occurs within the Sync Reset logic.

On the trailing edge of F2CLK, the unit address (bits 0 and 1 of word 2) is stored in the Unit Select Register, the disk command (bits 2 thru 4) is stored in the Disk Command Register, and the cylinder address (bits 07 thru 15) and two flag bits (bits 05 and 06) are loaded into the Cylinder Register. The shift/load (S/L) input to the Cylinder Register is presently low to cause a parallel load when it is clocked because the Field Counter does not equal CY or TS field at this time. The cylinder-head-sector address is now contained within the controller.

As in the first DMA cycle, the trailing edge of STB increments the DMA Initialization Sequencer to FAA3 and the DMA Address Register is incremented.

3.3.2.3 Third DMA Cycle (Disk Control Block)

As in the second DMA cycle (3.3.2.2), the DMA State Sequencer is once again started. The third word is extracted from Memory and placed on the D bus. F3CLK clocks the Command Busy (CMBSY) flip-flop, setting it if the contents of the Disk Command Register indicate any disk command other than NOOP. (NOOP does not allow the disk controller to go busy.) With the CMBSY flip-flop set, CBUSY goes true to indicate a busy status for the controller. Also at F3CLK time, the contents of the D bus, which contains the DMA word count (768 for this description), are loaded into the DMA Word Counter. As in previous cycles the trailing edge of STB increments the DMA Address Register and the DMA Initialization Sequencer to FAA4.

3.3.2.4 Fourth DMA Cycle (Disk Control Block)

As in previous cycles, the DMA State Sequencer is started to extract the fourth word from Memory. The information, which is the starting DMA address, is placed on the D bus. During Q3 time of the DMA State Sequencer, the information is clocked into the DMA Address Register by the leading edge of MACK. If the Disk Command Register contains a NOOP command the leading edge of STB will reset the Initialization Sequencer ending the operation and causing the controller to go to a quiescent state. Because, for this operation, the Disk Command Register will contain a Write Data Command (WD) the Initialization Sequencer will not be reset.

The second state of the DMA State Sequencer (Q1, Q2, Q3-) causes the RQ, REQ, and START flip-flop to be reset as in the previous cycles, but FAA4 does not directly set the RQ flip-flop as did FAA1, FAA2, and FAA3. This ends the "burst" mode operation.

Because the Disk Command Register did not contain a NOOP the Initialization Sequencer is incremented to DEXEC by the trailing edge of STB. The Initialization Sequencer remains in this state until termination of the operation. Sequencing of the controller is now turned over to the Disk Control Counter in the Control Function.

3.3.2.5 Sync Control Transfer

DEXEC going true causes the SF flip-flop to be set on the trailing edge of the next JKCLK2 pulse. The SF flip-flop stays set for one bit time to transfer control of the disk controller from the DMA Initialization Sequencer to the Disk Control Counter, and to perform other tasks described below.

The SF signal is applied to the Head Address Comparator to enable storage of a Head Address error if the head address contained in the Head Register is greater than the maximum numbered head. The Head Address Comparator has two functions; to indicate a Head Address error at the beginning of an operation (when SF goes true) and to indicate when the maximum numbered head is being used (for end-of-cylinder detection). It does this by comparing the number of the maximum numbered head (as assigned by rear-edge connector J11 strapping) to the contents of the Head Register (TR00 thru TR04). During Head Address error detection, the TR00 bit is not considered for comparison. It is disabled by the SF signal which causes the TR0IN and TR0IN- signals to be true, resulting in a high and a low being applied to the A=B IN and A≤B IN inputs respectively, to the comparator circuit. These are two of the three cascading inputs. (The other, A≥B IN, is tied to ground and need not be considered.) With A=B IN high, the indication is any less significant bits than the ones considered in the immediate circuit are equal. Therefore, only the more significant bits in this circuit need to be considered. Since static input 4 STRAP- has been grounded for this discussion, a high is applied to the B0 input. If a head address of 3 was contained in the Head Register, TR01 would be high, A0 would equal B0, and the A>B output would be low to indicate no head address error. However, if the head address was 4, TR02 would be high. TR02 is applied to the A1 input, and since B1 is grounded, A would be greater than B, and the A>B output (HAERR signal) would go high to indicate an error. When the SF signal goes high, it is ANDed with HAERR to set the Head Address Error (HAERF) flip-flop on the next clock pulse. Since Head 1 has been addressed for this description, no error occurs and the operation proceeds normally.

The Head Select Register is loaded on the trailing-edge of SF. The TR00 and TR01 bits from the Head Sector Register are clocked into the HSEL0 and HSEL1 flip-flop respectively (HSEL0 is the LSB and HSEL1 is the MSB). This occurs immediately before DC0 goes low due to the greater delays associated with the incrementing of the Disk Control Counter as compared to the delays associated with SF. The contents of the Head Select Register are sent to the selected disk drive to enable the specified head (Head 1 for this description).

Transfer of control from the DMA Initialization Sequencer to the Disk Control (DC) Counter is accomplished by enabling the counter to be increment from DC0 to DC1. SF and DC0 in the Increment logic causes DCS2- to go true and enable incrementation on the leading edge of the SRCLK pulse (trailing edge of JKCLK). DCS2- also provides a load signal to the Bit/Byte (B/B) Counter to enable presetting the counter to 3 bytes (2's complement of 24 bits). The SF signal enables the LD2 signal in the B/B Counter Loading logic, which subsequently enables the LD4 and LD8 signals (refer to table 3-4). These three signals provide the appropriate preset input signals to the B/B Counter to load 3 bytes. Since presetting the B/B Counter is synchronous with the clock input, the appropriate bits are loaded into the B/B Counter on the leading edge of the next SRCLK pulse (same one that increments DC Counter). The 3 byte times are required for synchronizing the transmission of the cylinder address strobe (SCA), and, if more than 4 heads are used, the head address strobe (SHA).

3.3.3 Disk Control Counter = DC1 (Figure 3-10)

The B/B Counter is incremented by one each bit time on the leading edge of the SRCLK pulse. When the B/B Counter has been incremented to a decode of BYTE0 (after 16 bit times from start of counting), DC1 and BYTE0 enable the C1 inputs to the Output Bus Mux. These are CF15 thru CF08 from the Cylinder Register which are the least significant eight bits of the nine-bit cylinder address. The output signals from the Output Bus Mux (OTBS0 thru OTBS7) carry these bits of the cylinder address to all on-line disk drives, but only the selected unit will input the information when the cylinder strobe is enabled. DC1 and BYTE0 also gate out the CF07 bit of the Cylinder Register (CAE) to the disk drives. CF07 is the MSB of a nine-bit cylinder address. At a B/B Counter decode of 70 (first bit time during BYTE0), a "1" is applied to the J input of the Strobe Cylinder Address (SCA) flip-flop. The flip-flop is set on the next clock pulse and the SCA signal is sent to the selected disk drive to strobe in the cylinder address. The disk drive then transmits an address acknowledge (ADACK) signal to indicate it has accepted the cylinder address and is starting the seek operation. ADACK and DC1 allow the ADAK1 flip-flop to set. ADAK1, DC1, and 00 (B/B Counter equals all "1"s) allow the DCS3 flip-flop to set on the trailing edge of the JKCLK. The SCA flip-flop is reset at the same time removing SCA from the disk drive. The next negative edge of the JKCLK (positive edge of SRCLK) enables the DC Counter to be incremented to DC2 and loads the B/B Counter. DC1 produces the LD1 signal in the B/B Counter Loading logic, which enables LD8 and LD4. These three signals provide the appropriate preset input signals to load 1 byte. The 1 byte time allows the disk drive time to respond and the response signal to settle (if a response is sent immediately due to seek error or heads already at specified cylinder) before the response is processed.

3.3.4 Disk Control Counter = DC2

In DC2, the disk controller waits for a response from the selected disk drive. If the heads do not reach the specified cylinder, the disk drive will respond with the seek error (SEEKER) signal. SEEKER is applied to the DC Counter Reset logic to enable the DCCL signal which synchronous resets the DC Counter (to DC0) to terminate the operation. DCCL is also applied to the Busy logic where it causes the Controller Reset (CONRS) flip-flop to set. CONRS enables the CBSYRS- signal which direct resets the CMBSY flip-flop and causes the DMA Initialization Sequencer to be reset to zero. CBUSY then goes false to indicate the controller is idle. Assuming no seek error, the controller simply awaits the seek complete signal from the selected disk drive.

Assuming Unit 0 was selected, and Cylinder 100 was addressed, the seek complete, Unit 0 (SCOM0) signal goes true when the heads in Unit 0 arrive at Cylinder 100. (In the "standard" configuration, SCOM0 is true when high.) The signal is inverted and applied to the polarity correction network, emerging as the ASCOM0 to be applied to the C0 input of the Seek Complete Multiplexer. Since Unit 0 is selected, the 0 input to the mux is applied to the output, causing the SEKCOM signal to go true. SEKCOM, DC2, and 00 produce DCS1 which enables incrementation of the DC Counter on the next SRCLK pulse. DCS1 provides the load signal to the B/B Counter to preset it to 1 byte on the next clock pulse. Since the DC Counter equals DC2, the LD1 signal in the B/B Counter Loading logic is enabled, which enables LD8 and LD4. These three signals provide the appropriate preset input signals to load 1 byte (eight bit times). At the start of DC3 time, information from the disk drive (Index or Sector mark) will not be processed until the 1-byte time has passed.

The ASCOM0 signal which enabled the SEKCOM signal output of the Seek Complete Multiplexer is stored in the Seek Complete Drive 0 (SCD0) flip-flop. This is done by ANDing ASCOM0 with the output of the Seek Complete Status Enable 0 (SCSE0) flip-flop which was set when the cylinder address was strobed into Unit 0. This applied a high to the J input of SCD0 which is then set on the next clock pulse. The output of SCD0 is available to the Processor by sense or status input. SCD0 direct resets the SCSE0 flip-flop.

3.3.5 Disk Control Counter = DC3

During DC3 the controller is waiting for an appropriate starting point for a sector search. Upon entering DC3, the previous sector was recognized or a sync reset has occurred [due to a platter change (refer to 3.3.2.1) or a unit change (refer to 3.3.2.2)] . If a sync reset has occurred, it is necessary to await an index mark (INDXB) to clear the SYNRS flip-flop (leading edge of INDXB) before sector marks can be received. INDXB direct sets the Divide-by-Two (DV2Q) flip-flop causing DV2Q to go high. The first raw sector mark after the index mark (beginning of Sector 0) allows the Sector Pulse flip-flop to be set on the trailing edge of JKCLK and reset when SECTX goes false generating a sector pulse (SECTB). The next JKCLK resets the Index Pulse flip-flop (INDEX) which was set by INDXB upon removal of the sync reset (SYNRS).

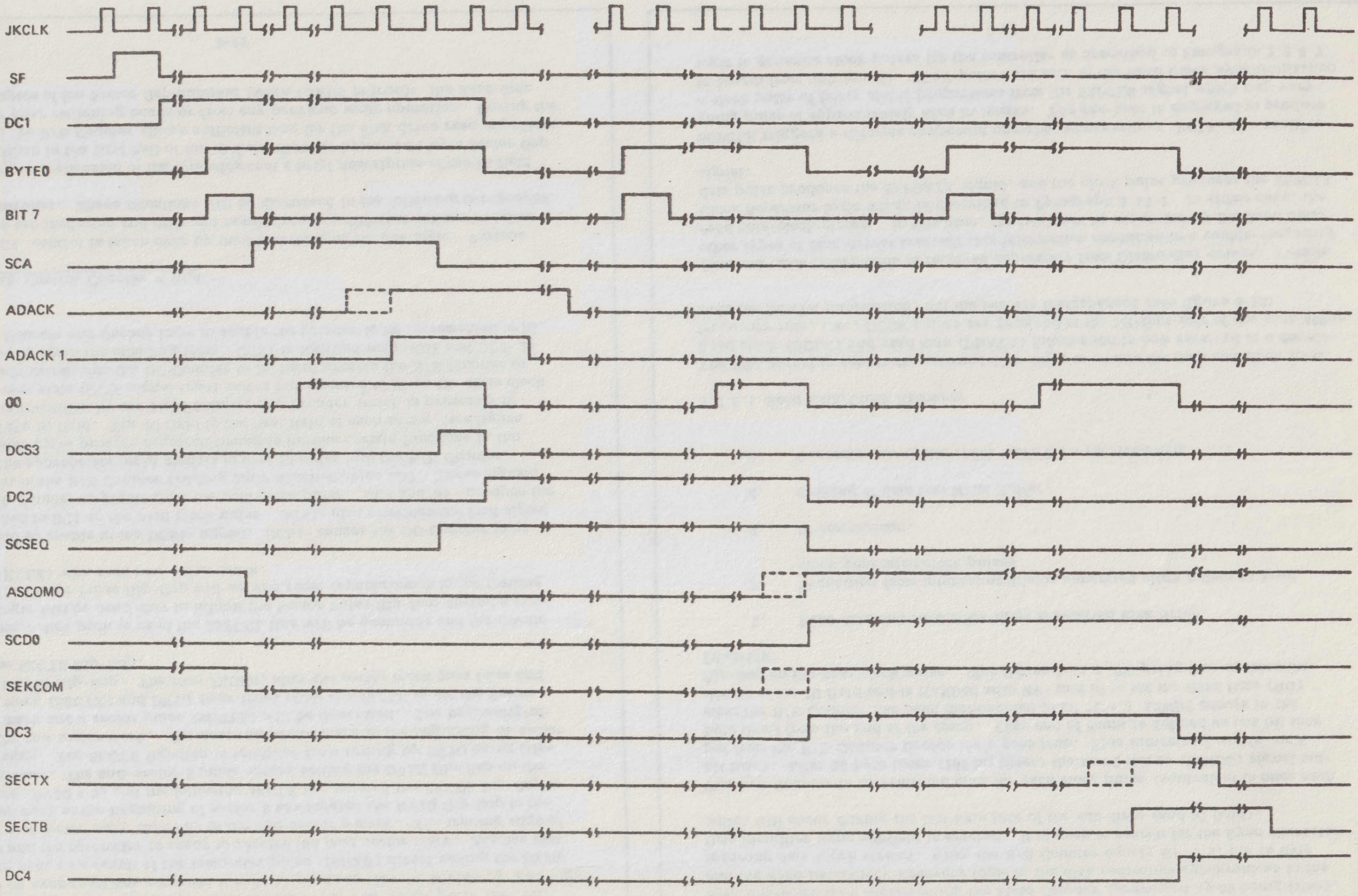

JKCLK
SF
DC1
BYTE0
BIT 7
SCA
ADACK
ADACK 1
00
DCS3
DC2
SCSEQ
ASCOMO
SCD0
SEKCOM
DC3
SECTX
SECTB
DC4

Figure 3-10. Disk Control Counter (DC0-DC3)

Assume that no sync reset (SYNRS) has occurred and the previous sector was recognized. If a 24 sector disk pack is being used the clock input to the Divide by Two flip-flop (2 SECCL) will be jumpered to the buffered, raw sector pulse (SECTX). Because no sync reset has occurred it must be assumed that the Divide-by-Two logic will be in sync as a result of the last index pulse (INDXB) direct setting the DV2Q flip-flop and the controller is ready to receive the next sector mark. Assume that the next raw sector mark (SECTX) is the mid-sector 8 mark. The trailing edge of the sector mark at the beginning of sector 8 has toggled the DV2Q flip-flop to the reset state (DV2Q = 0) and the following JKCLK has toggled the SECTB flip-flop to the reset state. The mid-sector 8 pulse occurs setting the DV2Q flip-flop on the trailing edge. The SECTB flip-flop is inhibited from setting by DV2Q being false during the raw sector mark. The next raw sector mark is the beginning-of-sector 9 sector mark and a sector pulse (SECTB) will be generated. The beginning-of-sector 9 mark (SECTX) and DV2Q (now true) allow the JKCLK to set the Sector Pulse (SECTB) flip-flop. The next JKCLK, after the sector mark goes false and resets the SECTB flip-flop.

If a 12 sector disk pack is used the 2SECCL line will be grounded and the Divide by Two logic will be used only to inhibit the Sector Pulse flip-flop during a sync reset. The Sector Pulse flip-flop will set and reset (synchronous to the trailing edge of JKCLK) with each raw sector mark.

SECTB and 00 enable to the DCS1- signal. DCS1- causes the DC Counter to be incremented to DC4 on the next clock pulse. DCS1- also provides the load signal to the B/B Counter to preset it on the next clock pulse. DC3 and WF- produce the LD6 signal in the B/B Counter Loading logic which enables LD7. These signals provide the appropriate input signals to load 24 bytes into the B/B Counter. Twenty-four bytes provide required timing to initiate certain functions in the middle of the IG field. The IG field is the first field of each sector (see figure 3-4). It is identified by the Field Counter and Decoder which is presently in the quiescent state (QUIE signal true) and is incremented to IG on the same clock pulse which increments the DC Counter to DC4 and presets the B/B Counter to 24. DCS1- is again the enabling term. DCS1 is NANDed with QUIE and DC2- in the Field Counter and Decode logic to enable the counter to be incremented to IG.

3.3.6 Disk Control Counter = DC4

During DC4, control is taken over by the Field Counter Decode logic. Various operations are instituted and different results require different actions be taken by the controller. These situations will be discussed in the following paragraphs.

For better comprehension of the following text a brief description of the IG field follows. When in the first half of the IG field (first 20 bytes of 24-byte Sector Gap sub-field) the B/B Counter allows sufficient time for the disk drive read amplifiers to recover after switching heads or from any previous write operation. During the last four bytes of the Sector Gap Subfield (when L2WDS is true): the Read Gate (RG) is turned on to allow the disk drive data recovery circuits to stabilize, the data from the drive is ignored to prevent the detection of an accidently generated Sync character from incrementing the Field Counter (prevented by 00 being false), and the Read Data/Clock Recovery logic in the disk controller synchronizes to the incoming data/clock stream. When the B/B Counter equals all "1"s, the 16 byte time Identifier Sync subfield is entered. It is used to search for the Sync character which will occur during the last byte time of the sub-field (and IG field).

The B/B Counter is incremented once for each clock pulse (equivalent to once each bit time). After 20 byte times (160 bit times) the last 2 words (L2WDS) signal output from the B/B Counter Decode logic goes true. This indicates 2 words, or 4 byte times from the end of the count. (The end of count is defined as one bit time after the B/B Counter has been incremented to all "1"s.) L2WDS occurs in the middle of the IG field and is NANDed with WF- and IG to set the Read Gate (RG) flip-flop on the next clock pulse. (See figure 3-11.) RG going true enables the following:

1. Read data and read clock lines at selected disk drive.
2. Transition from internal oscillator generated clock pulses to Read clock generated clock pulses.
3. ID comparison.
4. Shifting of data into Write Buffer.
5. Generate new cyclic check word from received data.

3.3.6.1 Read Data/Clock Recovery

The RGA signal is sent to the selected disk drive to enable the data and clock lines. Read clock (DCLK) and read data (DDATA) information is now received at a double-frequency rate, i.e., DCLK pulses are received at the bit-time rate of one each 400ns, as is the DDATA information, but the two are interspersed (see figure 3-12).

Data and clock information is received separately from Diablo disk drives. Certain other types of disk drives transmit this information combined in a double-frequency read data/clock stream. In this case, the two must be separated by the Read Data/Clock Separator logic which is described in Paragraph 3.13.1. In either case, the data pulse produces the SEPDATA signal, and the clock pulse produces the SEPCLK signal.

SEPCLK triggers a discrete component one-shot whose output, RCLK, is a positive going pulse of approximately 62ns in length. The one-shot is employed to produce a clock pulse of fairly stable proportions from the SEPCLK signal which may vary in length from unit to unit. RCLK pulses are sent to the Read Clock Synchronization logic to generate clock pulses for the controller as described in Paragraph 3.3.6.2.

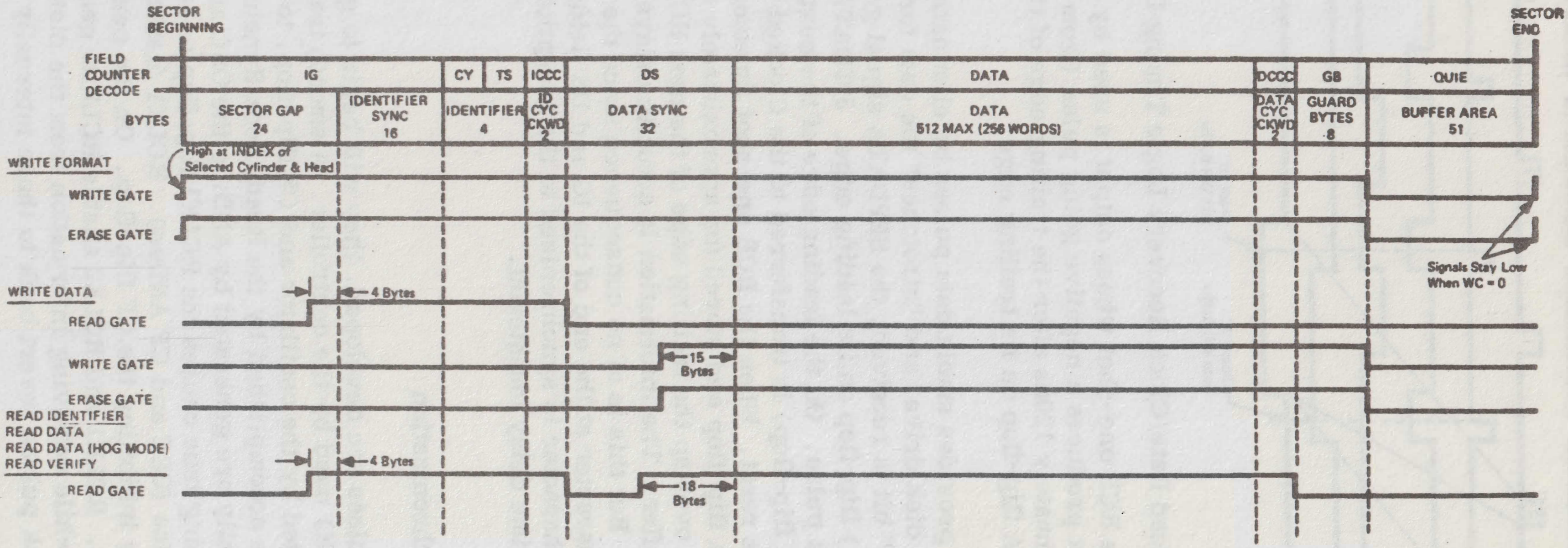

SECTOR BEGINNING
SECTOR END
FIELD COUNTER DECODE
IG
CY
TS
ICCC
DS
DATA
DCCC
GB
QUIE
BYTES
SECTOR GAP 24
IDENTIFIER SYNC 16
IDENTIFIER 4
ID CYC CKWD 2
DATA SYNC 32
DATA 512 MAX (256 WORDS)
DATA CYC CKWD 2
GUARD BYTES 8
BUFFER AREA 51
WRITE FORMAT
High at INDEX of Selected Cylinder & Head
WRITE GATE
ERASE GATE
Signals Stay Low When WC = 0
WRITE DATA
READ GATE
4 Bytes
WRITE GATE
15 Bytes
ERASE GATE
READ IDENTIFIER
READ DATA
READ DATA (HOG MODE)
READ VERIFY
READ GATE
4 Bytes
18 Bytes

Figure 3-11. Read, Write, and Erase Gate Timing

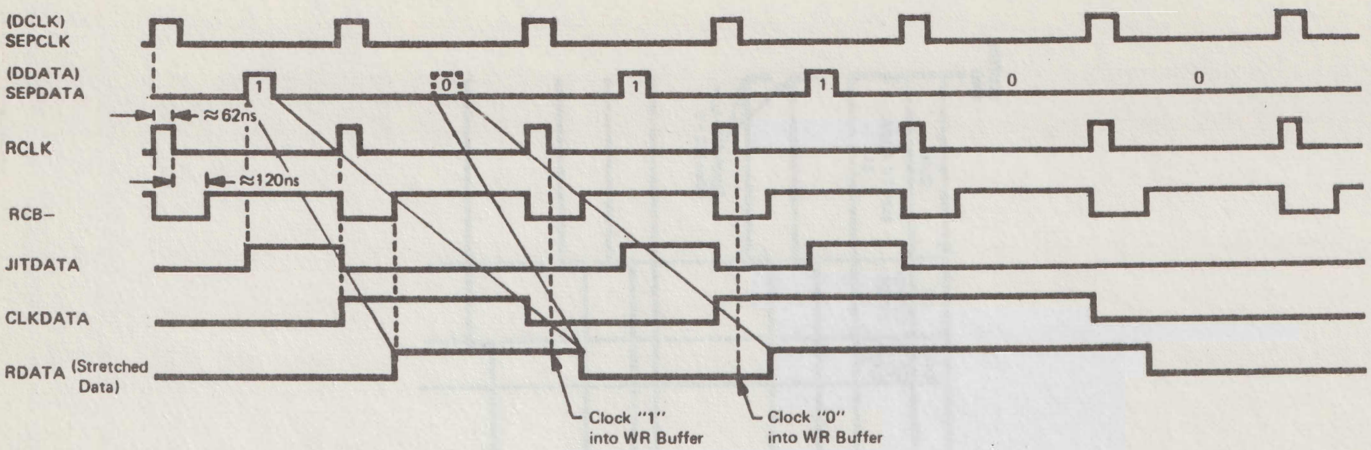


Figure 3-12. Read Data/Clock Recovery Logic Timing Diagram

SEPCLK also triggers the RCB one-shot whose output is used by the Data Recovery logic. The RCB one-shot produces a negative going pulse (from Q- output) which is set to time-out approximately 120ns after the trailing edge of the RCLK pulse. RCB- triggers the RDATA flip-flop on its trailing edge.

The Data Recovery logic provides stable data pulses by eliminating jitter from the pulses received from the disk drive, and "stretches" the data for coincidence with clock pulses. When a "1" bit is received, the SEPDATA signal goes true and clocks the Jitter Data (JITDATA) flip-flop on its leading edge. JITDATA stores the occurrence of an incoming data pulse. On the leading edge of the next RCLK pulse, the "1" (now in the JITDATA flip-flop) is transferred to the Clocked Data (CLKDATA) flip-flop, and JITDATA is reset. When the RCB one-shot times out, the "1" bit is transferred to the RDATA flip-flop and stored for approximately 400ns. The data bit is thus "stretched" to overlap the trailing edge of the next RCLK pulse which it shifts into the Write Buffer. The information is actually delayed one bit-time by the Data Recovery logic. But this is of no consequence since the controller is synchronized by the Sync character at the end of the IG and DS fields. All information received after the Sync character is synchronized to the reception of those characters, thus making the one bit-time delay immaterial.

3.3.6.2 Read Clock Synchronization

As Read Clock (RCLK) pulses are developed, they will begin to generate the clock pulses (JKCLK and SRCLK) used by the controller. A smooth transition must occur from clock pulses generated by the oscillator and CF flip-flop, to those generated by the RCLK pulses. This is accomplished by the Read Clock Synchronizer. Clock pulses originating internally are generated by ANDing the OSC and CF signals (see figure 3-13). RG going true causes the RCLK1 flip-flop to set on the trailing edge of the next clock pulse (OSC and CF ANDed). RCLK1 disables generation of clock pulses internally by inhibiting the CF flip-flop. On the next RCLK pulse, the RCLK2 flip-flop is set. RCLK1 and RCLK2 enable RCLK to generate the JKCLK and SRCLK clock pulses while receiving information from the disk drive. At the end of the "read" period, clock pulses revert back to those internally generated. The

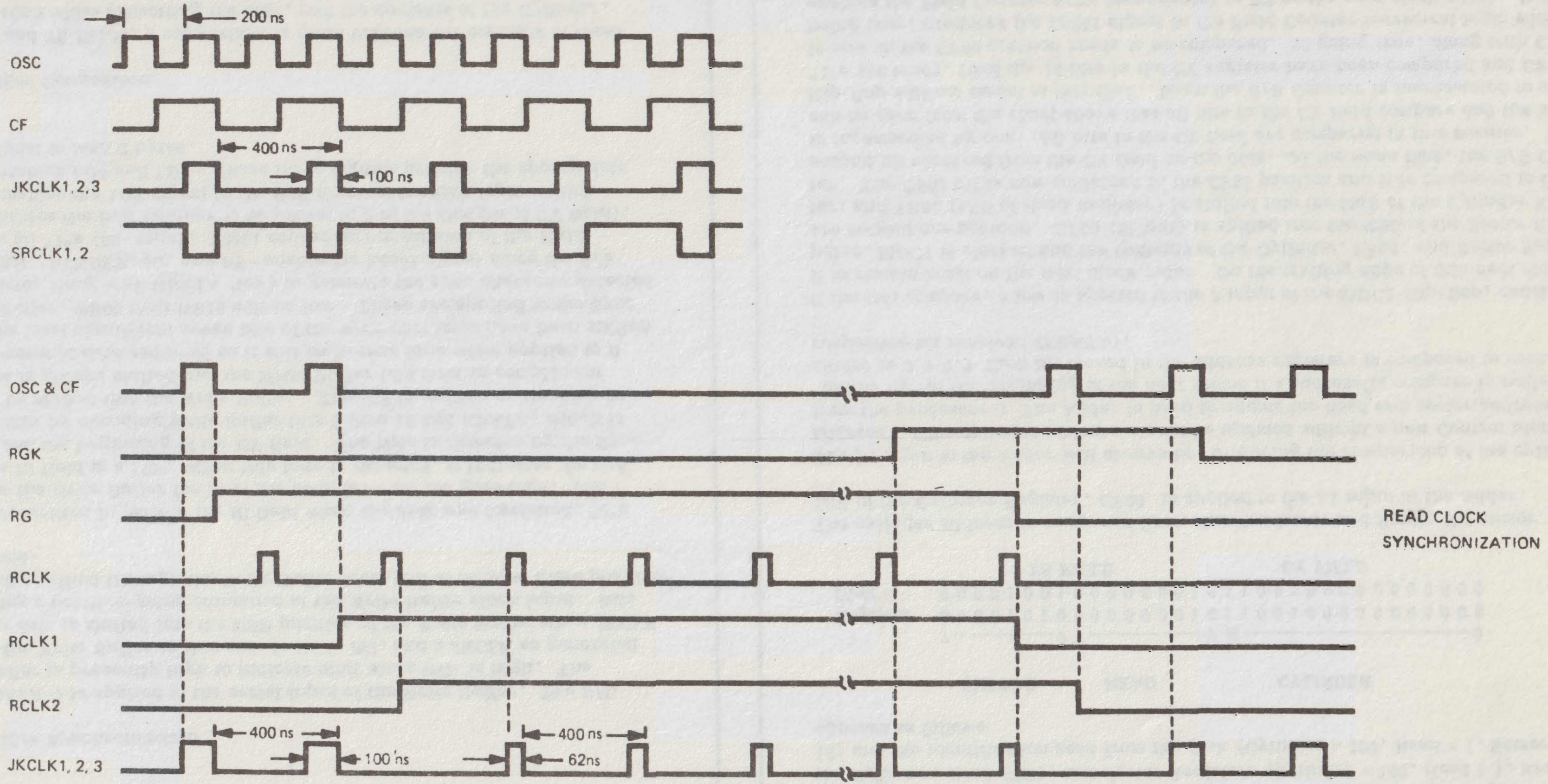

200 ns
OSC
CF
400 ns
100 ns
JKCLK1, 2, 3
SRCLK1, 2
OSC & CF
RGK
RG
RCLK
RCLK1
RCLK2
400 ns
100 ns
400 ns
62ns
JKCLK1, 2, 3
READ CLOCK
SYNCHRONIZATION

Figure 3-13. Clock Pulse Generation from Oscillator or RCLK

RGK signal goes true when the B/B Counter equals all "1"s (00) at the end of the ID or Data Cyclic Check Word fields. The RG and RCLK1 flip-flops are then reset on the next JKCLK clock pulse (externally generated). RGK goes low when the Field Counter is incremented to the next field. RCLK2 is then reset on the trailing edge of the next OSC and CF pulse. With RCLK1 and RCLK2 reset, clock pulses are once again generated from the internal source of OSC and CF.

3.3.6.3 Identifier Synchronization

Read data (RDATA-) is applied to the serial input of the Write Buffer. The S/L input to the buffer is presently high to indicate shift since WG- is high. The clock input to the Write Buffer in this case is DC4, RG, and a JKCLK as generated by RCLK. The data is shifted into the MSB position of the Write Buffer when JKCLK goes low causing a positive-going transition at the Write Buffer clock input. Bits are subsequently shifted through the Write Buffer from LSB to MSB on these positive-going transitions.

Since "0"s were written in most of the IG field when the disk was formatted, "0"s are shifted into the Write Buffer for 19 of the 20 bytes after RG goes true. The last byte in the IG field is a :7F. When this byte is detected, it indicates the end of the IG field and the beginning of the CY field. The byte is detected by the Sync Character detector by decoding Write Buffer bits 9 thru 15 and RDATA, which is the next bit to be shifted into the Write Buffer. The :7F is written on the disk as 01111111. Data is always shifted into the Write Buffer LSB first in complement form. (Complement of data required so it will be in true form when applied to D bus.) When the least significant seven bits of the sync character have been shifted into the Write Buffer, WB09 thru WB15 will be low. These are applied to the Sync Character Detector along with RDATA (low) to generate the sync character detected (SYNDET) signal. SYNDET, IG, and WF- enable the L6801 signal since the B/B Counter equals all "1"s (00- true). L6801 causes incrementation of the Field Counter and enables the B/B Counter to be preset to 2 bytes (length of CY field). IG being true enables the LD2 signal in the B/B Counter Loading logic, which subsequently enables LD4 and LD8. These three signals provide the appropriate preset input signal to load 2 bytes.

3.3.6.4 Identifier Comparison

During the CY and TS fields, a comparison is made between the contents of these fields, as recorded while formatting the disk, and the contents of the Cylinder, Head, and Sector Registers. If the two compare, the specified cylinder-head-sector is found and the Write operation can start. However, a comparison will not occur if the head is presently over Sector 9 and the sector desired is Sector 10. The comparison is made as follows:

The Sector ID Compare not (SIDC1-) flip-flop is reset during DC3. If this flip-flop is set at any time during the CY to TS fields, the indication is a false compare and the DC Counter reverts back to DC3 at the end of the Cyclic Check Word (ICCC) field. If SIDC1 remains reset, the indication is a positive comparison and writing will commence at the appropriate time. Assume the four bytes to be compared in the Cylinder, Head (TR), and Sector Registers (Cylinder = 100, Head = 1, Sector = 10) and the identification read from the disk (Cylinder = 100, Head = 1, Sector = 9) appears as follows:

```
              SECTOR          HEAD                CYLINDER

              7 ----------- 0 7 ----------- 0 15 ----------------------------- 0
Register      0 0 0 0 1 0 1 0 0 0 0 0 0 0 0 1 0 1 1 0 0 1 0 0 0 0 0 0 0 0 0 0
Disk          0 0 0 0 1 0 0 1 0 0 0 0 0 0 0 1 0 1 1 0 0 1 0 0 0 0 0 0 0 0 0 0
                          TS FIELD                        CY FIELD
```

The cylinder address is compared first, then the head, and finally the sector. The LSB of the Cylinder Register, CF00, is applied to the A1 input of the Adder.

The B1 input to the Adder will always be "0" during the comparison of the cylinder address. (The cylinder address cannot be updated without a new Control block from the processor.) The Adder is used to update the head and sector addresses "on the fly" at the beginning of the next sector if a successful compare is made. (Refer to 3.3.8.) Each bit stored in the address registers is compared to each respective bit received (RDATA).

If the two compare, a low is applied to the J input of the SIDC1-flip-flop, causing it to remain reset on the next clock pulse. On the trailing edge of this next clock pulse, SIDC1 is clocked and the contents of the Cylinder, Head, and Sector Registers are rotated one position. CF00 (SUM01) is shifted into the MSB of the Sector Register, and TR00 (LSB of Head Register) is shifted into the MSB of the Cylinder Register. The CF01 bit is now contained in the CF00 position and it is compared to the second bit received from the CY field on the disk. At the same time, the B/B Counter is incremented by one. All bits in the CY field are compared in this manner. It can be seen from the chart above that all bits in the CY field compare and the SIDC1-flip-flop will not be set at this time. When the B/B Counter is incremented to all "1"s (00 true), 15 of the 16 bits in the CY register have been compared and CF15 is now in the CF00 position ready to be compared. 00 going true, along with CY being true, produces the L6801 signal in the Field Counter increment logic which enables the Field Counter to be incremented to TS on the next clock pulse. It also enables the B/B Counter to be loaded with 2 bytes, the length of the TS field. LD2, LD4, and LD8 in the B/B Counter Loading logic are again enabled since the CY signal is presently true.

On the clock pulse, the Field Counter is incremented, the B/B Counter is loaded, and TR00 (LSB of Head Register) is shifted into the CF00 position for comparison. The Head Register is compared during the next eight bit times with the SIDC1- flip-flop remaining reset. When the LSB of the Sector Register is shifted into CF00, the false comparison is finally detected (in sector 9, searching for sector 10). SUM01 will be low at this time, and RDATA will be high. The output of the EX OR will go high, causing a high to be applied to the J input of the SIDC1-flip-flop. The flip-flop is then set on the next clock pulse to indicate "no compare." SIDC1- being set prevents the Sector ID Compare (SIDCOM) flip-flop from setting upon entering the ICCC field. The remainder of the bits in the Sector Register are also compared, but this is of no consequence. When the B/B Counter is incremented to all "1"s, L6801 again goes true enabling the Field Counter to be incremented to ICCC (IC Cyclic Check Word field) and the B/B Counter is loaded with 2 bytes, the length of the ICCC field. These events occur on the clock pulse and a final rotating shift is made in the Cylinder, Head, and Sector Registers to place the contents of these registers in their original positions.

During the CY and TS fields, a cyclic check word is developed in the Cyclic Check Word (CCW) Register from the contents of these fields. (Refer to Cyclic Check Word Register, paragraph 3.2.5.10.) During the ICCC field, this regenerated cyclic check word is compared to the contents of the ICCC field. This is done as follows: the contents of the CCW Register are shifted out from the LSB position (CCW00) one bit at a time on each clock pulse. The contents of the register are not rotated at this time, as they are when the cyclic check word is being developed. The contents are replaced with "0"s to clear the register for when the next cyclic check word is developed. CCW00 is applied to an EX OR gate associated with the Identifier and Data Cyclic Check Word Error detection circuits where it is compared to the corresponding bit being received from the ICCC field. If no ID compare error has occurred (SIDC1=1) and if any of the 16 bits of the field do not compare, the ID Cyclic Check Word Error (IDCCE) flip-flop is set. This would cause the DC Counter to reset to DC0 when the drive reached the end of the sector (DC5) if a successful comparison (SIDCOM=1) was made. In this particular case, since the comparison was unsuccessful (SIDCOM=0), the sector operation would simply continue by returning to DC3. (Refer to figure 3-14.) The IDCCE flip-flop cannot set to cause termination unless a successful ID compare occurs (SIDC1=1).

Since the SIDCOM flip-flop was not set because of the "no compare" condition (SIDC1 set), the DCCLD signal in the DC Counter Load 3 logic is enabled at the end of the ICCC field. This causes the DC Counter to be preset to DC3 and the Field Counter to be reset to QUIE. Also, the RG flip-flop is reset at this time to disable the data and clock lines from the disk drive, and cause the controller to revert back to internally generated clock pulses.

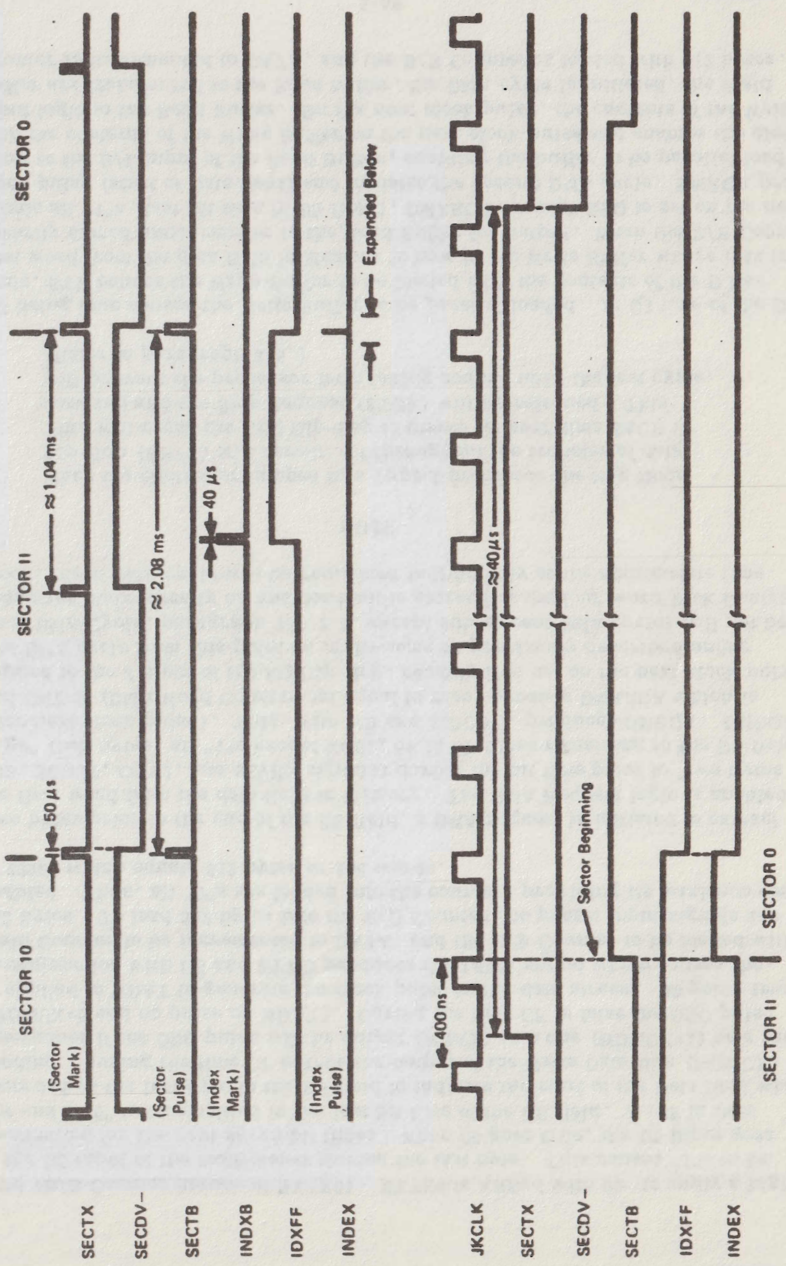


Figure 3-14. Index and Sector Pulse Timing

3.3.7 Disk Control Counter = DC4 (ID Compare-Sector 10)

In DC3, the SIDC1-flip-flop is reset to prepare for the next ID comparison. Nothing further occurs until a Sector pulse is developed to indicate the start of Sector 10 (Figure 3-3). When the pulse occurs, the DC Counter is incremented to DC4, the Field Counter is incremented to IG, and the B/B Counter is loaded with 24 bytes. The operation through the IG, CY, and TS fields is exactly the same as previously described, except that a successful ID comparison is made this time. Since the head is presently over Sector 10 and the addressed sector is also 10, all bits in the Cylinder, Head, and Sector Registers compare to the corresponding bits from the disk, and the SIDC1 flip-flop is not set. On the first clock pulse after the Field Counter is incremented to ICCC, the Sector ID Compare (SIDCOM) flip-flop is set to indicate the successful comparison. Again during the ICCC field, the cyclic check word is compared for errors to cause termination by setting the IDCCE flip-flop if an error occurs. One bit-time from the end of the ICCC field, 00 goes true to produce the L6801 signal which causes the Field Counter to be incremented to DS, and the B/B Counter to be loaded with 32 bytes. LD4 is enabled in the B/B Counter Loading logic to provide the appropriate preset input signals to load the 32 bytes, which is the length of the DS field. Also at the end of the ICCC field, the RG flip-flop is reset to disable the Read Data and Read clock lines from the disk drive, and also to revert the controller back to internally generated clock pulses.

The following paragraph is applicable to the controller being installed in an LSI-1 processor. At the start of the Data Sync (DS) field the Hog Mode flip-flop (RHFF) is directly set. RHFF directly sets the REQ flip-flop causing a Stop Request (STOP) to be issued to the processor. The Stop Acknowledge (SACK) from the processor sets the START flip-flop making DPOT go false. The DMA Cycle does not start (DMA State Sequencer inhibited) until the RQ flip-flop is set by DMARQA going true at the end of the DS field (when writing) or the beginning of the Data field. The processor does not regain control until the DMA Word Counter goes to zero. (Refer to paragraph 3.5.)

In the Data Sync (DS) field, the B/B Counter is incremented on each clock pulse, but nothing more occurs until one byte past the mid-point. This point is determined by a decode of 015 (byte 15, bit 0) from the B/B Counter. This signal goes true 15 byte times plus 1 bit time from the end of the DS field. On the next clock pulse, the Write Gate (WG) flip-flop is set. This causes the WGA and EGA signals to go true and enable the write and erase currents respectively in the selected disk drive. (Erase head follows the Write head and is only used to trim the written data to specifications - approximately .007 inch.)

Information now begins to be written on the disk. The information is transmitted to the disk drive in a double-frequency data/clock stream format (see figure 3-15). During the DS field, the information to be transmitted is applied to the D5 input of the Write Data Multiplexer. Zeros are transmitted until the last byte of the DS field (B/B Counter decode of BYTE0). BYTE0 is ANDed with 00- to apply a high to the D5 input of the multiplexer during the last byte. This causes "1"s to be transmitted for the next seven bit times. When 00 goes true, the D5 input goes low and a "0" is transmitted in the last bit time of the DS field. A : 7F is thus recorded as the last byte in the DS field to indicate the start of the Data field when reading. During the time CF is true the output of the Write Data Mux (WDMUX) determines if the OSC pulse will be output (WDAT) as a one (WDMUX=1) or a zero (WDMUX=0 and no pulse on WDAT). During the time CF is false the OSC pulse is applied to WDAT to generate the clock pulse in the data stream. 00 going true, in conjunction with DS and WFWD produces the L6801 signal which causes the Field Counter to be incremented to DATA. and the B/B Counter to be loaded with 512 bytes. To load 512 bytes into the B/B Counter, no preset input signals are enabled. Thus, all "0"s are loaded into the counter, providing its maximum count of 4096, which equals 512 bytes or 256 words.

Two bytes prior to the end of the DS field, a DMA request is initiated to extract the first word from the data field in Memory. The DMA Request logic is enabled (DS, 2COY1, COY2, and 0EVEN signals) during the bit time prior to "two bytes to go" (two bytes, all "1"s except YC01, or 16 bit times remaining in the DS field after next clock pulse). This, with WD and SIDCOM, produces DMRQA. DMRQA and CNT=0- (DMA Word Counter not equal to zero) produce DMARQA which is applied to the J input of the RQ flip-flop, causing it to set on the next clock pulse. The DMA cycle from this point on is the same as previsouly described under First DMA Cycle, paragraph 3.3.2.1, except subsequent DMA cycles will not be requested automatically as was done while extracting the four-word Disk Control block. Each DMA cycle will be requested individually at the appropriate time.

NOTE

> When the controller is used in a Type 1 processor the Hog Mode flip-flop (RHFF) will remain set throughout the transfer of data. This will cause the REQ flip-flop to direct set each time SACK is removed and the Stop Request (STOP) will be reissued. This will prevent the processor from taking control until the last cycle. (Refer to paragraph 3.5.)

WG being true causes the Write Buffer to be parallel loaded. At Q3 time of the DMA cycle, STB causes the Write Buffer to be loaded with the contents of the D bus. The first word from the data field in Memory is now in the Write Buffer where it is temporarily stored until transfer to the Read Buffer for output. When the B/B Counter equals all "1"s (last bit time in DS field), DMARQA, causes REQ to set on the next clock pulse (start of Data field) and initiates the second DMA cycle. DMRQA provide a low to the S/L input of the Read Buffer, enabling the buffer to be parallel loaded with the contents of the Write Buffer on the next clock pulse and enables the clock input logic to the Read Buffer. On the next clock pulse, the contents of the Write Buffer are transferred to the Read buffer, the DMA cycle is initiated, the Field Counter is incremented to DATA, and the B/B Counter is loaded with 512 bytes.

3.3.7.1 Data Field

With the Field Counter equal to DATA (FC01, 02, and 03 output signals from the Field Counter equal 110 respectively), the D6 input to the Write Data Multiplexer is enabled. This is the LSB of the Read Buffer (RB00). The multiplexer output, WDMUX, OSC, and CF produce the data portion of the double-frequency data/clock stream (WDAT). The clock pulse portion of the data/clock stream is produced at the center of the bit time, by OSC and CF-. (Refer to timing diagram figure 3-15 below.) Data and clock pulses are thus sent to the disk and recorded.

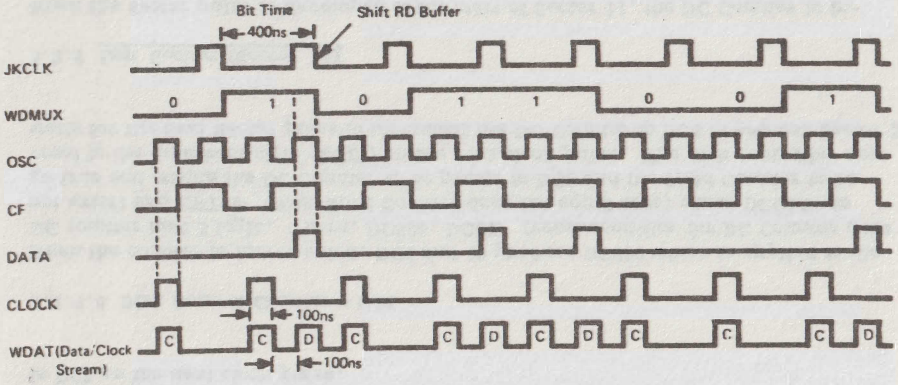


Figure 3-15. Data/Clock Stream Format, Timing Diagram

The WDMUX signal is also applied to the Cyclic Check Word (CCW) Register to begin developing the cyclic check word for the Data field. WDMUX, WG and DCCC- (DCCC- disables continued generation of the cyclic check word during the DCCC field) are applied to an EX OR gate whose other input is the LSB of the CCW Register (CCW00). The output of the EX OR is applied to the A input of the CCW Register, which is one leg of a 2-input internal NAND gate, utilized as the serial input to the register. The other leg, input B, enables the internal NAND gate only during the CY, TS, DATA, and DCCC fields.

NOTE

> During the IG, ICCC, and DS fields, "0"s are shifted into the register to clear it, and during GB and QUIE, the clock pulse input to the register is disabled to provide cyclic check word availability to the Processor, if required.

The generated bit for the cyclic check word is shifted into the register on the clock pulse. Thus, after 16 bit times, the even parity cyclic check word has been generated for the first word; after 32 bit times, for the first and second word; and so on throughout the Data field. (Refer to Cyclic Check Word Register, paragraph 3.2.5.10, for more information on the cyclic check word.)

After the first data bit is transmitted, the Read Buffer is shifted one position to bring the next bit to the RB00 position for transmission. The S/L input to the Read Buffer is presently high to enable shifting since the DMRQA signal is presently false. DMRQA only goes true when the last bit of each word is being transmitted to enable parallel loading of the Read Buffer, and to request another DMA cycle. DMRQA is enabled during the Data field by L2WDS-, DATA, and 0EVEN. Clock pulses for Read Buffer are developed by DATA, JKCLK3, and WD.

The Write operation continues in the previously described manner until 254 words are transmitted, at which time the L2WDS signal goes true. This is a decode of the B/B Counter indicating two words, or 32 bit times remain in the Data field. When L2WDS goes true, the last DMA cycle is being initiated. (L2WDS disables DMRQA.) The DMA cycle extracts the last word from the memory data field and stores it in the Write Buffer. As with all the other data words, this last word must also be transferred to the Read Buffer for transmission after the last bit of the previous word is transmitted. DMRQA normally provides the low to the S/L input of the Read Buffer to enable parallel loading. It will not be available this time, however, since no further DMA requests will be made. For the last parallel transfer from the Write Buffer to the Read Buffer, the low is produced by L2WDS, WD, SIDCOM, DATA, YC01-, and 0EVEN. The last two words are loaded into the Read Buffer and transmitted to the disk drive to be recorded in the Data field of Sector 10.

When 00 goes true (while transmitting the last bit of the Data field), L6801 is once again produced to enable the Field Counter to be incremented to DCCC, and the B/B Counter to be loaded with 2 bytes, on the next clock pulse. LD2, LD4, and LD8 are enabled in the B/B Counter Loading logic to provide the appropriate preset input signals to load 2 bytes.

3.3.7.2 Data Cyclic Check Word Field

With the Field Counter equal to DCCC (FC01, 02 and 03 equal to 111) the D7 input to the Write Data Mulitplexer is enabled. This is the LSB position of the CCW Register (CCW00). The cyclic check word is transmitted to the disk drive in the same double-frequency data/clock stream as data. The contents of the CCW Register are rotated while being transmitted. This is to provide availability of the cyclic check word to the Processor during the GB and QUIE states of the Field Counter, if required. The contents of the CCW Register are unchanged while being rotated since further generation of the cyclic check word has been disabled by DCCC- at the serial input to CCW Register.

When the last bit of the cyclic check word is being transmitted, L6801 goes true to enable the Field Counter to be incremented to GB, and the B/B Counter to be loaded with 8 bytes. The LD2, LD4, and LD8 signals in the B/B Counter Loading logic are enabled to provide the appropriate preset input signals to load 8 bytes.

3.3.7.3 Guard Bytes Field

The Guard Bytes field provides sufficient distance between the DCCC field and the head when the write and erase currents are turned off to ensure no noise spikes will occur in that field. Zeros are written in the GB field because the D0 input to the Write Data Multiplexer is presently enabled (select inputs FC01, 02 and 03 equal 0 0 0), providing a steady low at the output (WDMUX signal low).

During the last bit time of the GB field, 00, GB and WD produce WGK in the K input logic of the WG flip-flop. This causes the flip-flop to reset on the next clock pulse and disables the write and erase currents at the disk drive. Also during the last bit time of the GB field, 00 with DC4 and GB enable incrementation of the DC Counter to DC5 on the next clock pulse.

3.3.7.4 Disk Control Counter = DC5

When the counter is incremented, DC5 and 00 produce DC500 which is applied to the DC counter load 3 logic. There, DC500, DCCL- (reset condition for DC Counter does not exist) and CNT=0- (DMA Word Counter does not equal zero) cause DCCLD- to go true and enable the DC Counter to be preset to DC3 and the Field Counter to be reset to the quiescent state (QUIE) on the next clock pulse. The disk controller now waits for the next Sector pulse to increment the DC Counter to DC4 to process Sector 11.

3.3.8 Last Sector (Sector 11)

When the Sector pulse is developed at the start of Sector 11, the DC Counter is incremented to DC4, the Field Counter is incremented to IG, and the B/B Counter is loaded with 24 bytes, all as previously described (Refer to paragraph 3.3.5). The operation proceeds normally through the IG field. The Field Counter is then incremented to CY where a successful comparison of the cylinder address results. When in the TS field, the head address is also compared successfully. The Sector address, however, will not compare successfully unless the contents of the Sector Register, presently 10, are incremented to 11. Incrementation of the Sector Register occurs simultaneously with its comparison to the sector address recorded on the disk. The Adder logic does this in the following manner. When the final bit of the Head Register (bit TR07) is being compared, B/B Counter decode 01 goes true. This enables the J input logic of the Carry flip-flop (TS, 01, SIDCOM, and SECCOM- are all true). The flip-flop is then set on the next clock pulse, resulting in the B1 input to the Adder going high. CF00 (presently the LSB of the Sector Register) is low, resulting in the Adder output, SUM01, going high. This now compares to the LSB of the sector address recorded on the disk (see below).

```
0 0 0 0 1 0 1 0 Sector register = 10
              1 Carry
0 0 0 0 1 0 1 1 Result = 11
0 0 0 0 1 0 1 1 Recorded on disk
```

SUM01, TS and BIT0- (not the last bit time in TS field) reset the Carry flip-flop on the next clock pulse. The remaining bits of the Sector Register are then compared without alteration. Had the result of the addition been "O" (SUM01 low), the Carry flip-flop would not have been reset and its output would have been added to the next bit. In this manner, the carry ripples through the contents of the Sector Register to appropriately update each bit for comparison and subsequent storage. A successful comparison results, the SIDC1- flip-flop is not set, and the SIDCOM flip-flop remains set to indicate a successful comparison for Sector 11.

When the incremented contents of the Sector Register are back in their original positions, the SECM1 output from the Last Sector Comparator goes true. The comparator compares the least significant five bits of the Sector Register to static input signals SS00- thru SS04- from rear-edge connector J11 which indicate the assigned maximum numbered sector. Assuming 11 has been assigned as the maximum numbere sector, the A=B output of the comparator, SECM1, goes true. SECM1 is applied to the J input of the Last Sector Complete (SECCOM) flip-flop where it causes the flip-flop to be set during the DCCC field of Sector 11.

The operation now proceeds normally through the ICCC, DS, and Data fields. The middle one-third of the 768 word data field in Memory is extracted as previously described and recorded in the Data field of Sector 11. On the first clock pulse in the DCCC field, the SECCOM flip-flop is set. SECCOM going true has several functions, each of which is described below, as it occurs. The operation then proceeds normally through the DCCC and GB fields. At the end of the GB field, the DC Counter is once again incremented to DC5. DC5, SECCOM, 00, and JKCLK3 produce the TRS- signal which clears the Sector Register. The Sector Register is now equal to Sector 0, the next sector to be processed. The Sector 0 to be processed, however, is not associated with the head presently selected which is Head 1. The output of the Head Select Register enables the selected head, therefore it must be incremented to select Head 2. TRS clocks the Head Select Register and the inputs to the Head Select Register are controlled by the two LSB's of the Head (TR) Sector Register, and DC0. In the J input logic of the Head Select 1 (HSEL1) flip-flop, TR01, presently low, is EX ORed with the AND of TR00 and DC0-. The result is a high and a low being applied to the J and K inputs respectively, of HSEL1. TR00, presently high, and DC0 are EX ORed to apply a low and a high to the J and K inputs respectively, of HSEL0.

On the trailing edge of TRS, HSEL1 (MSB) is set, and HSEL0 (LSB) is reset. The contents of the register now disable Head 1 and enable Head 2 at the disk drive. The contents of the Head (TR) Register must also be changed to reflect the switching of heads. This will be done later during the TS field of Sector 0.

Since Head 2 is associated with a different platter than Head 1, the source of Index and Sector marks will be different. The disk controller must be synchronized to this new source. (Refer to paragraph 3.3.5.)

3.3.9 Sector 0

To regress slightly, in Sector 11 when the DC Counter was incremented to DC5, it was again preset to DC3 and the Field Counter was reset to QUIE on the next clock pulse. The Counters remain in these states until the Index pulse is developed from the new source. At that time, the DC Counter is incremented to DC4, the Field Counter to IG, and the B/B Counter is loaded with 24 bytes, all as previously described. The operation continues normally through the IG field and into the CY field. At the end of the CY field when the last bit of the cylinder address is being compared, CY, 00, SECCOM (last sector complete), and SIDCOM are NANDed in the J input logic of the Carry flip-flop. This will cause the Carry flip-flop to set on the next clock pulse and increment the contents of the Head (TR) Register to 2 in the same manner as previously described when the Sector Register was incremented from 10 to 11. A successful comparison is thus made on the head address. With the contents of the Sector Register having been previously reset to zero during DC5 of Sector 11, a successful comparison is also made on the sector address. SECCOM being true at this time prevents the carry flip-flop from being set and thus prevents the Sector register from being incremented. (SECCOM is reset in DC4 time when in the DCCC field.) The operation then proceeds through the ICCC, DS, and Data fields as previously described.

The last 256 words of the 768 words contained in the data field of Memory are written in the Data field of Sector 0. During the last DMA cycle to extract the last word from the data field in Memory, the DMA Word Counter is decremented to zero. When the DC Counter is incremented to DC5 at the end of the GB field, DC500 and CNT=0 enable the DCCL- signal. This causes the DC Counter to be reset to DC0 on the next clock pulse. At the same time, CNT=0- and DEXEC in the Busy logic set the Controller Reset (CONRS) flip-flop. CONRS- enables the CBSYRS- signal which direct resets the CMBSY flip-flop to place the disk controller in the idle state. CBSYRS- also resets the DMA Initialization Sequencer causing the DEXEC signal to go false.

3.3.10 Sense Controller Not Busy (SEN :F,0)

Sense commands using a function code of 0 or 1 can be issued during the Write operation to determine its completion. When the controller goes idle, the CBUSY- input to the Sense Multiplexer goes high to cause a not busy response when the Sense command is issued. (Refer to paragraph 3.3.1 for a more detailed description of the Sense operation.)

3.3.11 Status Input (INA :F,0)

Status is input to the Processor by issuing an Input command with a device address of :F and a function code of 0. When the device address is decoded, ADDR goes true and is ANDed with IN to produce INADR. (See mnemonic description in appendix A for location of signal source.) INADR and AFB01- and 02- enable the output of the I/O Data Bus Multiplexer. This enables the multiplexer output for any Input command executed by the disk controller which uses a function code of 0 or 1. AB00 is applied to the SEL input of the mulitplexer. Since a function code of 0 is being used, AB00 is low. This enables the A inputs to the multiplexer, which are the status inputs. Status is thus applied to the D bus and sent to the Processor.

In the Status Reset logic, the Status Reset signal (STRST-) is generated by Function Code 0, IN, APLS, and CBUSY- during the latter half of the Input command. STRST- resets the following status or interrupt store flip-flops and counter:

PHALT
RATER
Timeout counter
HAERF
IDCCE
DACCE
EOC
IDCOME
SCD0 THRU SCD3

With the completion of Status input, the Write operation is complete.

3.4 READ DATA OPERATION (Figure 3-16)

The Read Data operation is essentially the same as the Write Data operation previously described. The four-word Disk Control block must be extracted from Memory, the specified cylinder must be found, the appropriate head must be enabled, and the specified sector must be identified. Therefore, a thorough understanding of the Write Data operation is essential for proper understanding of the Read Data operation. Only those protions of the operation which differ from the Write Data operation will be described in detail. Assume only the first 100 of the possible 256 words in the Data field of the specified sector will be read.

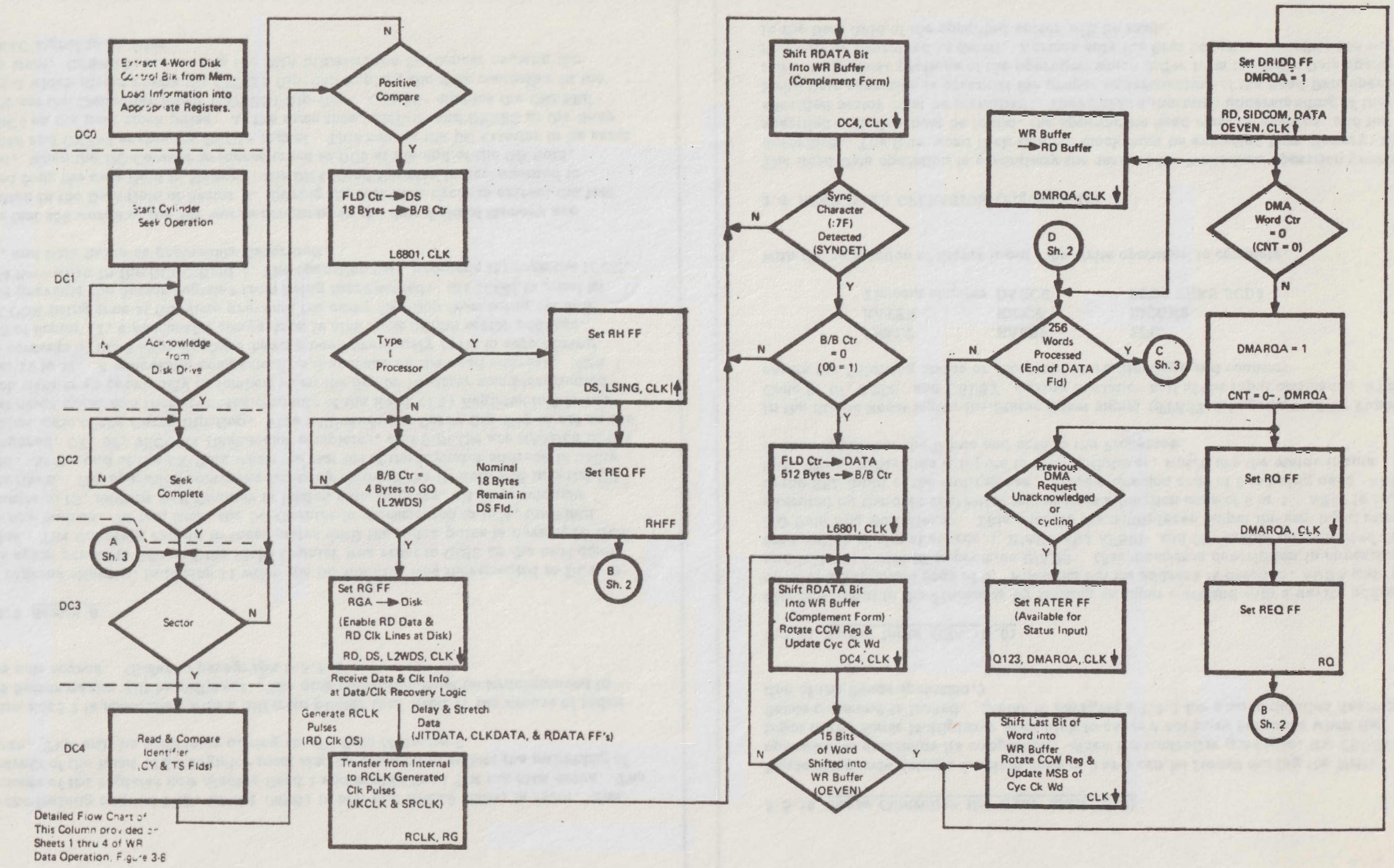

Extract 4-Word Disk
Control Blk from Mem.
Load Information into
Appropriate Registers.
DC0
Start Cylinder
Seek Operation
DC1
Acknowledge
from
Disk Drive
N
Y
DC2
Seek
Complete
N
Y
A
Sh. 3
DC3
Sector
N
Y
DC4
Read & Compare
Identifier
(CY & TS Flds)
Detailed Flow Chart of
This Column provided on
Sheets 1 thru 4 of WR
Data Operation, Figure 3-8
N
Positive
Compare
Y
FLD Ctr → DS
18 Bytes → B/B Ctr
L6801, CLK
Type
I
Processor
Y
N
B/B Ctr =
4 Bytes to GO
(L2WDS)
N
Nominal
18 Bytes
Remain in
DS Fld.
Y
Set RG FF
RGA → Disk
(Enable RD Data &
RD Clk Lines at Disk)
RD, DS, L2WDS, CLK
Receive Data & Clk Info
at Data/Clk Recovery Logic
Generate RCLK
Pulses
(RD Clk OS)
Delay & Stretch
Data
(JITDATA, CLKDATA, & RDATA FF's)
Transfer from Internal
to RCLK Generated
Clk Pulses
(JKCLK & SRCLK)
RCLK, RG
Set RH FF
DS, LSING, CLK
Set REQ FF
RHFF
B
Sh. 2
Shift RDATA Bit
Into WR Buffer
(Complement Form)
DC4, CLK
Sync
Character
(:7F)
Detected
(SYNDET)
N
Y
B/B Ctr
= 0
(00 = 1)
N
Y
FLD Ctr → DATA
512 Bytes → B/B Ctr
L6801, CLK
Shift RDATA Bit
Into WR Buffer
(Complement Form)
Rotate CCW Reg &
Update Cyc Ck Wd
DC4, CLK
15 Bits
of Word
Shifted into
WR Buffer
(OEVEN)
N
Y
WR Buffer
→ RD Buffer
DMRQA, CLK
D
Sh. 2
256
Words
Processed
(End of DATA
Fld)
N
Y
C
Sh. 3
Previous
DMA
Request
Unacknowledged
or
cycling
Y
Set RATER FF
(Available for
Status Input)
Q123, DMARQA, CLK
Shift Last Bit of
Word into
WR Buffer
Rotate CCW Reg &
Update MSB of
Cyc Ck Wd
CLK
Set DRIDD FF
DMRQA = 1
RD, SIDCOM, DATA
OEVEN, CLK
DMA
Word Ctr
= 0
(CNT = 0)
N
DMARQA = 1
CNT = 0–, DMRQA
Set RQ FF
DMARQA, CLK
Set REQ FF
RQ
B
Sh. 2

Figure 3-16. Read Data Operation Flow Chart
(Sheet 1)

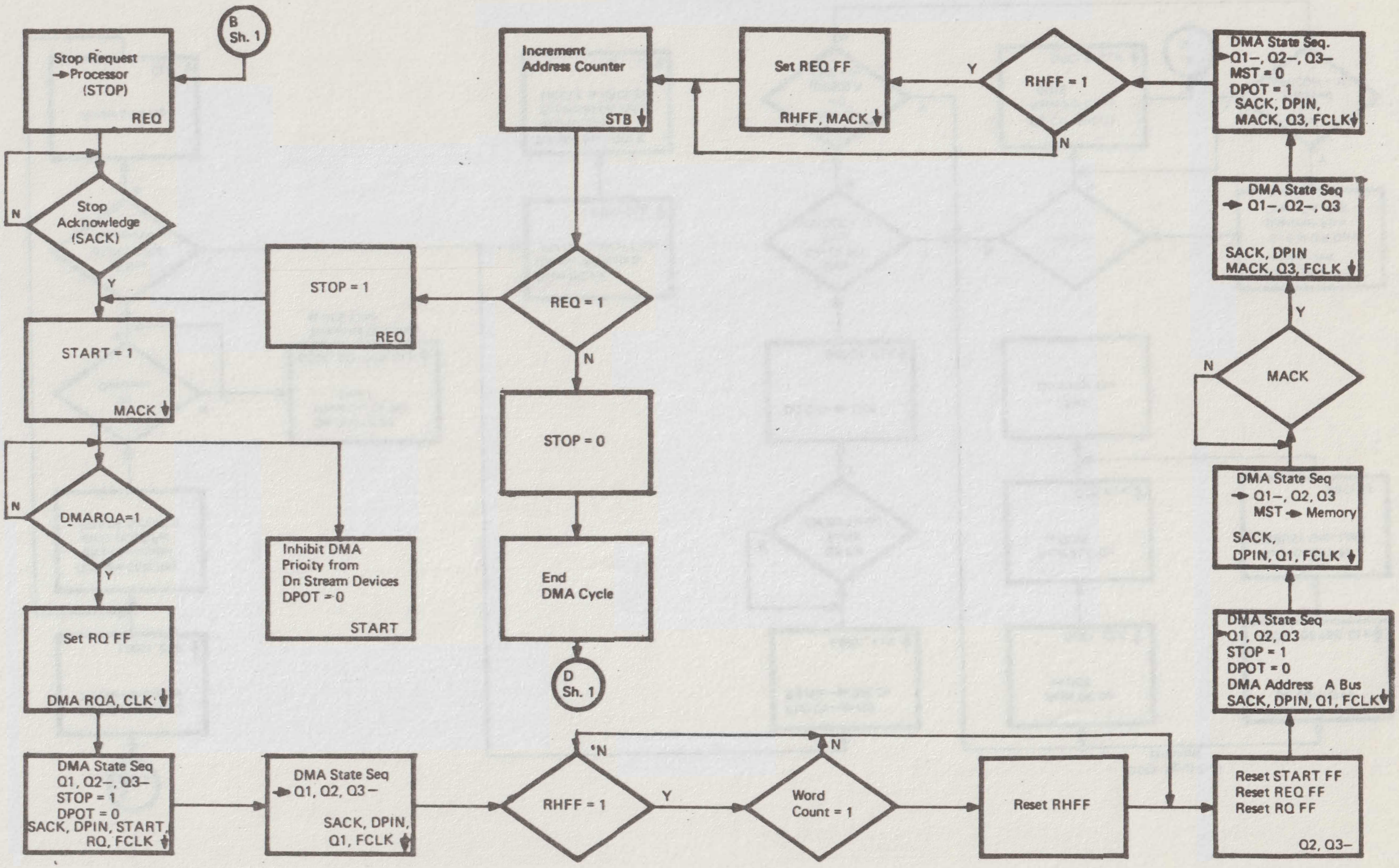

B
Sh. 1
Stop Request
→ Processor
(STOP)
REQ
Stop
Acknowledge
(SACK)
N
Y
START = 1
MACK ↓
DMARQA=1
N
Y
Set RQ FF
DMA RQA, CLK ↓
DMA State Seq
Q1, Q2–, Q3–
STOP = 1
DPOT = 0
SACK, DPIN, START,
RQ, FCLK ↓
STOP = 1
REQ
Inhibit DMA
Prioity from
Dn Stream Devices
DPOT = 0
START
DMA State Seq
→ Q1, Q2, Q3 –
SACK, DPIN,
Q1, FCLK ↓
Increment
Address Counter
STB ↓
REQ = 1
N
STOP = 0
End
DMA Cycle
D
Sh. 1
RHFF = 1
N
Y
Word
Count = 1
N
Set REQ FF
RHFF, MACK ↓
RHFF = 1
Y
N
Reset RHFF
DMA State Seq.
→ Q1–, Q2–, Q3–
MST = 0
DPOT = 1
SACK, DPIN,
MACK, Q3, FCLK ↓
DMA State Seq
→ Q1–, Q2–, Q3
SACK, DPIN
MACK, Q3, FCLK ↓
Y
MACK
N
DMA State Seq
→ Q1–, Q2, Q3
MST → Memory
SACK,
DPIN, Q1, FCLK ↓
DMA State Seq
→ Q1, Q2, Q3
STOP = 1
DPOT = 0
DMA Address A Bus
SACK, DPIN, Q1, FCLK ↓
Reset START FF
Reset REQ FF
Reset RQ FF
Q2, Q3–

Figure 3-16. Read Data Operation Flow Chart
(Sheet 2)

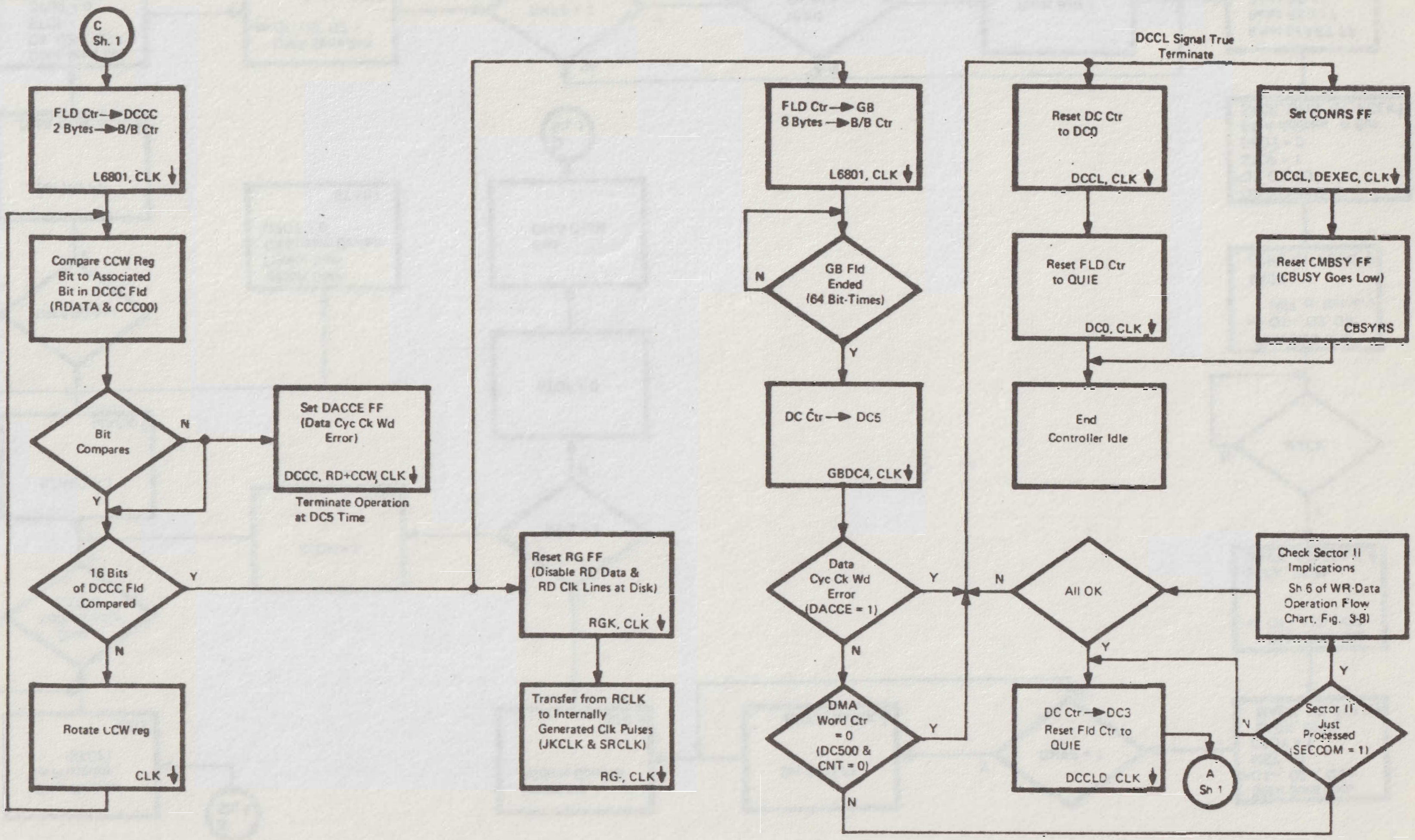

C
Sh. 1
FLD Ctr→DCCC
2 Bytes→B/B Ctr
L6801, CLK ↓
Compare CCW Reg
Bit to Associated
Bit in DCCC Fld
(RDATA & CCC00)
Bit
Compares
N
Y
Set DACCE FF
(Data Cyc Ck Wd
Error)
DCCC, RD+CCW, CLK ↓
Terminate Operation
at DC5 Time
16 Bits
of DCCC Fld
Compared
Y
N
Rotate CCW reg
CLK ↓
Reset RG FF
(Disable RD Data &
RD Clk Lines at Disk)
RGK, CLK ↓
Transfer from RCLK
to Internally
Generated Clk Pulses
(JKCLK & SRCLK)
RG-, CLK ↓
FLD Ctr→GB
8 Bytes→B/B Ctr
L6801, CLK ↓
N
GB Fld
Ended
(64 Bit-Times)
Y
DC Ctr→DC5
GBDC4, CLK ↓
Data
Cyc Ck Wd
Error
(DACCE = 1)
Y
N
DMA
Word Ctr
= 0
(DC500 &
CNT = 0)
Y
N
DCCL Signal True
Terminate
Reset DC Ctr
to DC0
DCCL, CLK ↓
Reset FLD Ctr
to QUIE
DC0, CLK ↓
End
Controller Idle
Set CONRS FF
DCCL, DEXEC, CLK ↓
Reset CMBSY FF
(CBUSY Goes Low)
CBSYRS
N
All OK
Y
Check Sector II
Implications
Sh 6 of WR-Data
Operation Flow
Chart, Fig. 3-8)
Y
Sector II
Just
Processed
(SECCOM = 1)
N
DC Ctr→DC3
Reset Fld Ctr to
QUIE
DCCLD CLK ↓
A
Sh 1

Figure 3-16. Read Data Operation Flow Chart
(Sheet 3)

The Read Data operation is initiated and the information contained in the four-word Disk Control block is stored in the appropriate disk controller registers (figure 3-9). The output of the Disk Command Register is decoded to produce the read enable RE signal which subsequently enables read data (RD). RD is used later in the operation to enable certain functions. After the Disk Control field is extracted from Memory, control is transferred to the DC Counter which is incremented through DC1 and DC2 for the cylinder seek operation. When seek complete is received from the selected disk drive, the DC Counter is incremented to DC3 to await a Sector pulse. Upon reception of the Sector pulse, the DC Counter is incremented to DC4 and the Field Counter is incremented to IG. Proceeding through the IG field, the RG flip-flop is set, at the end of 20 bytes, to enable reading (see figure 3-11). Information ("0"s) from the ID Sync portion of the IG field is then read and the Field Counter is incremented to CY when the sync character, :7F, is detected. The identifier is then read and compared in the CY and TS fields. Assume a positive comparison is made. The Field Counter is then incremented to ICCC, and at the end of the field, the RG flip-flop is reset and the Field Counter is incremented to DS. The controller will go into the "Hog" mode if a Type 1 processor is used (refer to paragraph 3.3.7).

Proceeding through the DS field, the RG flip-flop is once again set when 14 bytes into the field. At the beginning of the DS field, only 18 bytes are loaded into the B/B Counter. (DS field is 32 bytes long.) When L2WDS goes true, it is NANDed with RI+RD+RV and DS which causes RG to be set on the next clock pulse. Information ("0"s) is then received and shifted into the Write Buffer. When the sync character (SYNDET) is detected, the Field Counter is incremented to DATA and reception of data begins. Data is shifted into the Write Buffer in complement form. As the 15th bit of each data word is shifted into the Write Buffer, the 0EVEN signal goes true. 0VEN, SIDCOM, DATA, and RD in the DMA Request logic produce the read data DMA request (RDDRQ) signal (refer to figure 3-17). RDDRQ- being true causes the DMA Read or ID Request Delayed (DRIDD-) flip-flop to set on the next clock pulse, the same clock which shifts the last bit of each word into the Write Buffer. DRIDD- being true produces DMRQA which is then ANDed with CNT=0- to produce the DMARQA signal. DMARQA causes the RQ flip-flop to be set on the next clock pulse and initiate a DMA request as previously described (paragraph 3.3.2.1). The DMRQA signal provides a low at the S/L input of the Read Buffer to enable a parallel load from the Write Buffer. DMRQA is also NANDed with JKCLK3 to provide a clock pulse to the Read Buffer. The complete word contained in the Write Buffer is thus transferred to the Read Buffer on the next clock pulse, the same one which shifts the first bit (LSB) of the next word into the Write Buffer, and also sets the RQ flip-flop to initiate the DMA request. The controller then has 16 X 400ns, or 6.4μs to obtain the DMA cycle and transfer the contents of the Read Buffer to Memory. If a DMA cycle is not obtained within this time period, a Rate error will occur. If the DMA cycle is not complete (Q1, Q2, or Q3 set) when the DMARQ signal once again occurs to initiate the next DMA cycle, the Rate Error (RATER) flip-flop will set on the next clock pulse. The output of the flip-flop is available to the Processor through Status input. RATER will cause termination of the operation.

Assuming no Rate error, the Read Data operation continues similar to a write operation. During the Read Data operation, no Read Mode (RD) signal is issued to the Memory resulting in a quicker Memory Acknowledge (MACK).

Q3, WD-, and DC4 in the DMA Control Function logic produce data enable signal DEN2. This signal enables the bus drivers. As previously mentioned, the data is shifted into the Write Buffer in complemented form, and is thus transferred to the Read Buffer in complement form. If a particular bit in the buffer equals "1" (low), the associated driver applies a low to the D bus. The D bus is negative-true. If the bit equals "0" (High), a high is applied to the bus. When DEN2 goes false (low), the drivers are disabled and present a high impedance to the D bus.

During each DMA cycle, the DMA Word Counter is decremented by one and the DMA Address Register is incremented by one (trailing edge of Q3 time). When the DMA Word Counter has been decremented to zero (after 100 DMA cycles for this discussion), the counter equals zero (CNT=0). CNT=0 disables further generation of the DMARQA signal in the DMA Request logic each time DMRQA goes true. Thus, further DMA cycles are not initiated. Data words are still received for the duration of the Data field. They are still shifted into the Write Buffer and transferred to the Read Buffer, but they are not transferred to Memory since the required DMA cycles will not occur.

During this time of no data transfer to Memory, the cyclic check word for the Data field continues to be updated with the reception of each word. Upon completion of the Data field (after all 256 words have been read), the DCCC field is entered and the regenerated cyclic check word is compared to the contents of the DCCC field by the EX OR gate associated with the Identifier and Data Cyclic Check Word Error detection circuits. (Previously described under Identifier Comparison, paragraph 3.3.6.3.) If any of the bits contained in the Cyclic Check Word Register do not compare to the associated bit received from the DCCC field, the Data CCW Error flip-flop will be set. This will cause the DC Counter to be reset to DC0, and terminate the operation at the end of the sector (DC5 time). At the end of the DCCC field, RD, 00, and DCCC are NANDed to produce RGK in the Read Gate logic. RGK causes the RG flip-flop to reset on the next clock pulse and disable the Read Data and Read Clock lines from the disk drive. It also enables the controller to revert back to internally generated clock pulses. The controller then proceeds through the GB field. At the end of the GB field, the DC Counter is incremented to DC5. DC5 is ANDed with 00 and CNT=0 to produce the DCCL- signal in the DC Counter rest logic. This resets the counter to DC0 and causes the CONRS flip-flop to set on the next clock pulse. CONRS then resets the CMBSY flip-flop in the Busy logic. The Read Data operation is thus terminated and the controller goes idle.

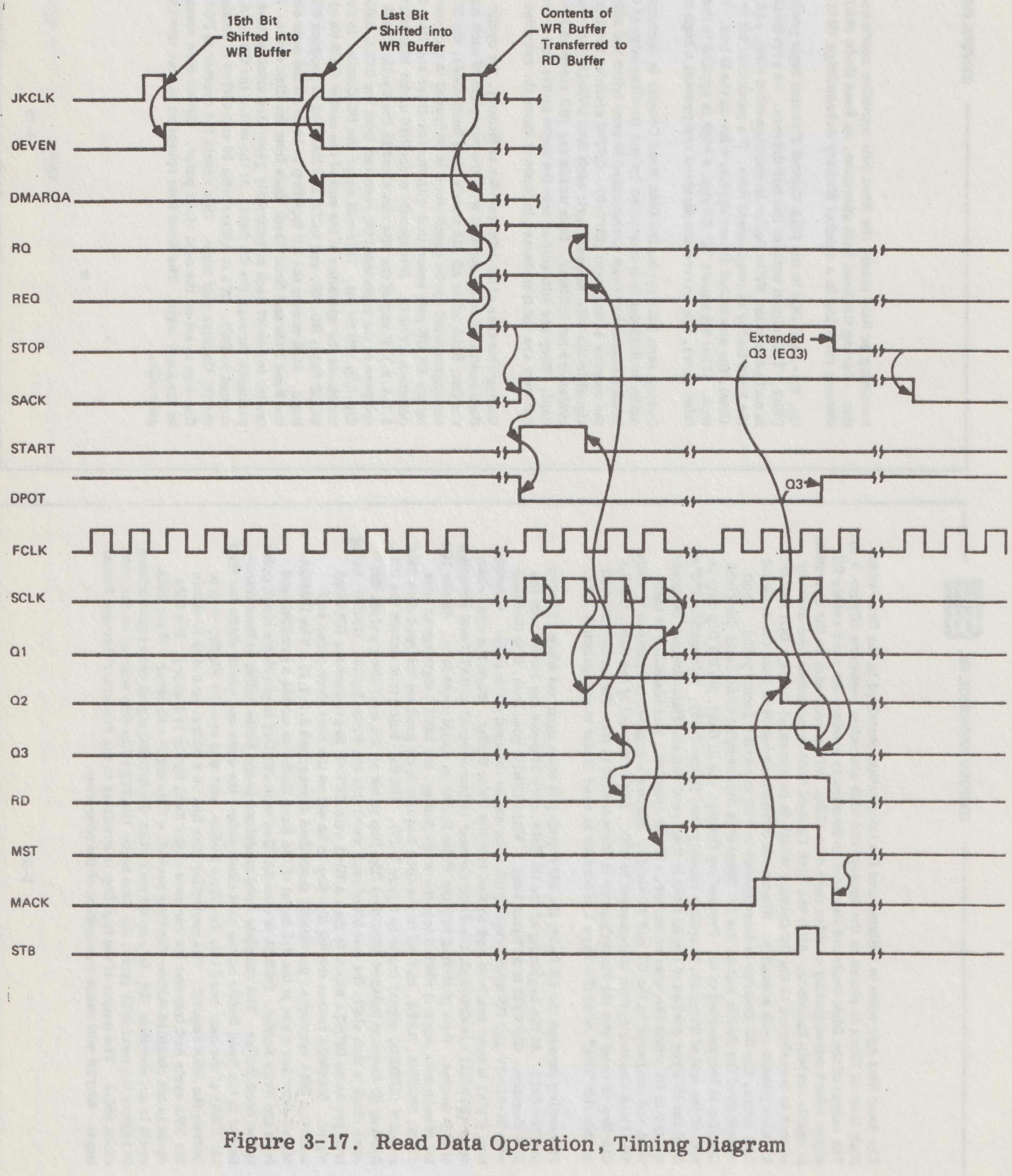

15th Bit Shifted into WR Buffer
Last Bit Shifted into WR Buffer
Contents of WR Buffer Transferred to RD Buffer
JKCLK
0EVEN
DMARQA
RQ
REQ
STOP
Extended Q3 (EQ3)
SACK
START
Q3
DPOT
FCLK
SCLK
Q1
Q2
Q3
RD
MST
MACK
STB

Figure 3-17. Read Data Operation, Timing Diagram

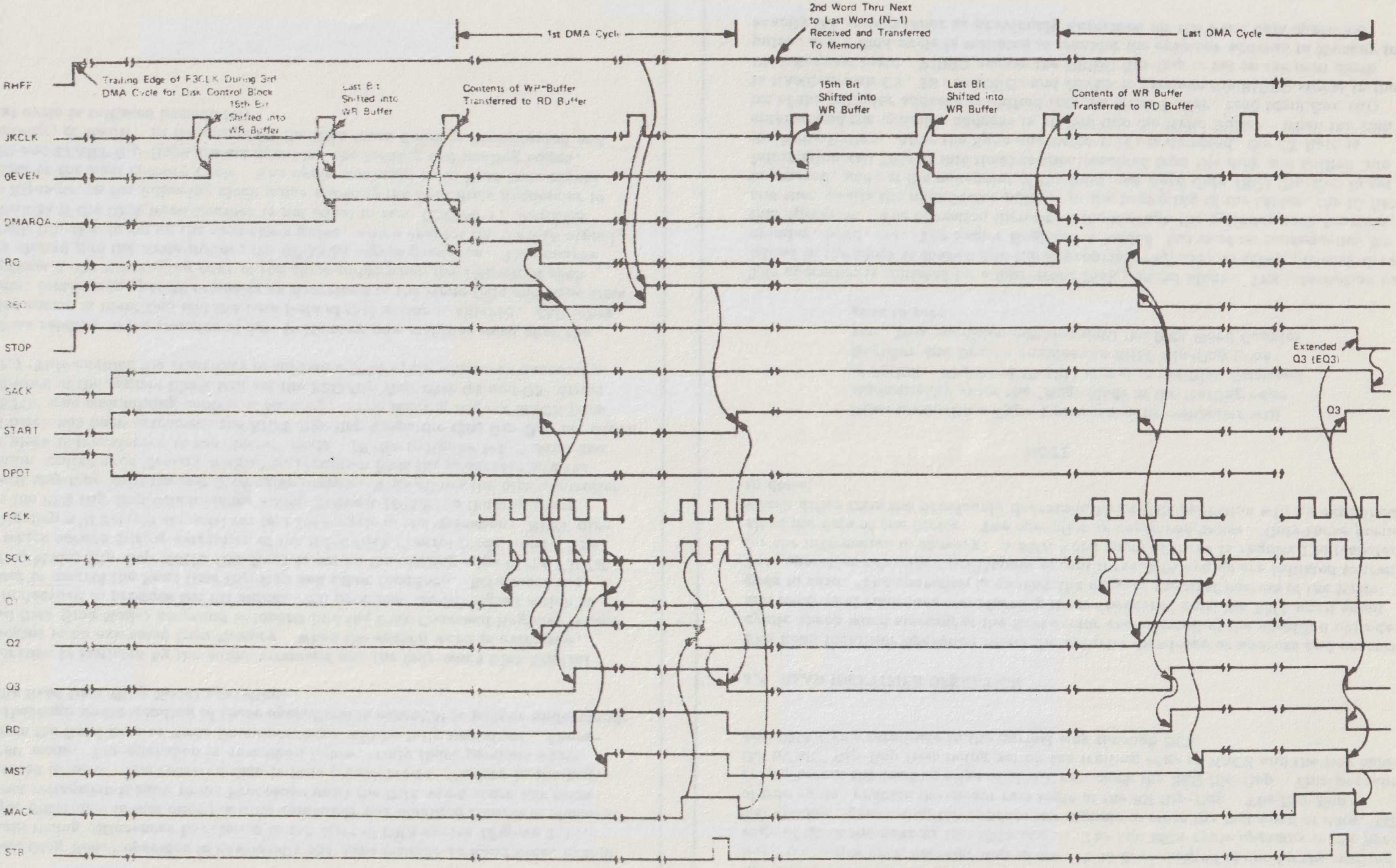

1st DMA Cycle
2nd Word Thru Next to Last Word (N–1) Received and Transferred To Memory
Last DMA Cycle
Trailing Edge of F3CLK During 3rd DMA Cycle for Disk Control Block
15th Bit Shifted into WR Buffer
Last Bit Shifted into WR Buffer
Contents of WR Buffer Transferred to RD Buffer
15th Bit Shifted into WR Buffer
Last Bit Shifted into WR Buffer
Contents of WR Buffer Transferred to RD Buffer
Extended Q3 (EQ3)
Q3
RHFF
JKCLK
OEVEN
DMAROA
RG
REQ
STOP
SACK
START
DPOT
FCLK
SCLK
Q1
Q2
Q3
RD
MST
MACK
STB

Figure 3-18. Read Hog Mode Operation Timing

3.5 READ DATA (HOG MODE) OPERATION

Read Data (Hog Mode) operates in essentially the same manner as Read Data, except for certain timing differences in relation to the start of DMA cycles (Figure 3-18.) The major difference is that once the disk controller has obtained control of Memory, it does not relinquish it back to the Processor until the DMA word count has been decremented to zero. The received data is thus transferred to Memory in the hog, or "burst" mode. The operation is described below. Only those portions which differ from the Read Data or Write Data operations will be fully explained. Therefore, a thorough understanding of those operations is essential to proper understanding of the Read Data (Hog Mode) operation.

The operation is initiated by the output command and the four-word Disk Control block begins to be extracted from Memory. When the second word is extracted, the Read Data (Hog Mode) command is loaded into the Disk Command Register whose output is decoded to produce the RH signal. RH produces the RD signal which is used later to control the Read Gate flip-flop and other functions. RH causes the Read (Hog Mode) flip-flop (RHFF flip-flop) to set on the trailing edge of the F3CLK pulse, which occurs during extraction of the third Disk Control block word. The RHFF flip-flop will remain set until the last DMA cycle of the operation. RHFF direct sets the REQ flip-flop which issues a Stop Request (STOP) to the processor. STOP will stay true until the last DMA cycle occurs. This allows the disk controller to maintain control over Memory without interruption from the processor and the control block is transferred in the "burst" mode. (Refer to figure 3-9.) After the control block has been extracted, the RHFF flip-flop keeps the REQ flip-flop set which keeps STOP true maintaining control of Memory. (The leading edge of MACK from the last word of the control block will set the REQ flip-flop after Q2 and Q3- direct reset it.) This enables the controller to initiate a DMA cycle whenever necessary.

Conditions relating to the transfer of data to Memory now stabilize until after the specified sector is identified and the Data field of that sector is entered. (All other functions, continue to operate normally as described in the Write Data and Read Data descriptions.) On the trailing edge of the clock pulse when the 15th bit of each word is shifted into the Write Buffer, the RDDRQA signal goes true. This causes the DRIDD flip-flop to set on the next clock pulse, which enables the DMRQA signal, and DMARQA if the DMA Word Counter is not equal to zero (CNT=0-). DMARQA causes RQ to set on the following clock pulse allowing the DMA State Sequencer to increment on the next memory cycle. The cycle continues as in Read Data except the REQ and START flip-flops are set again by the leading and trailing edges, respectively, of MACK. At the end of Q3 the DMA Word Count is decremented and the next cycle is initiated immediately.

This process of performing DMA cycles and enabling the appropriate conditions for the immediate initiation of the next cycle continuously repeats itself until the DMA word count has been decremented to one. It is decremented to one by the trailing edge of Q3 of the next-to-last DMA cycle. The last DMA cycle operates in the normal manner, generating the appropriate signals to store the last word of data. Q2 of this cycle, enables the direct rest logic of the RH flip-flop. The flip-flop is reset, before the leading edge of MACK can clock the REQ flip-flop. This prevents the START flip-flop from being set by the trailing edge of MACK and the Hog Mode and DMA Cycle terminate in the normal way through DC5.

3.6 READ IDENTIFIER OPERATION

The Read Identifier operation reads the cylinder-head-sector address and associated cyclic check word starting at the first sector encountered at the specified cylinder and head, and continues transferring these "headers" until the DMA word count goes to zero. The operation is exactly the same as the first portion of the Write Data operation described previously except three DMA cycles are initiated to transfer the information to Memory. A DMA word count of three is required to transfer all of the data of one sector. The operation is described below. Only those portions which differ from the previously described Write Data operation will be explained in detail.

NOTE

> When used with a Type 1 processor the controller will automatically enter the "Hog" Mode at the trailing edge of F3CLK. The Read ID (RI) signal in the Disk Command Register and Decode enables the RHFF flip-flop to be set. This condition remains until the DMA Word Counter goes to zero.

The operation is initiated by a four-word Disk Control block. The information contained in the block is loaded into the appropriate registers to select the disk drive, cyinder, head, etc. The Sector Register is loaded, but is of no consequence for this operation. The operation then proceeds through the cylinder seek function, and then awaits the next Sector pulse. At the beginning of the sector, the IG field is entered, and, at the mid-point of the field, the Read Gate (RG) flip-flop is set. Information (all "0"s at this time) is then received from the disk and shifted into the Write Buffer. After the Sync character (:7F) is detected, the CY field is entered and the cylinder address is shifted into the Write Buffer. When the 15th bit of the cylinder address is shifted into the Write Buffer, read identifier (RI) is NANDed with CY, TS, or ICCC, and 0EVEN to produce the RIDRQ signal in the DMA Request logic. RIDRQ causes the DRIDD flip-flop to set on the next clock pulse, and a DMA cycle is initiated to transfer the cylinder address to Memory in exactly the same manner as previously described for the Read Data operation.

(Refer to Read Data operation, timing diagram figure 3-17.) During the DMA cycle, the DMA address is incremented by one and the DMA word count is decremented by one. At the end of the CY field, the TS field is entered: the head and sector addresses are shifted into the Write Buffer: the RDATA is read into the Adder to be shifted into the Head Sector Register; and the CARRY flip-flop input is disabled to prevent updating of the RDATA as it is shifted into the Head Sector Register. This allows the Head Select Register to be updated and valid end-of-cylinder information to be obtained. RI inhibits the input to the SIDCI- flip-flop insuring an SIDCOM with each "header." When the 15th bit of the TS field is shifted into the Write Buffer, RIDRQ again goes true to set the DRIDD flip-flop on the next clock pulse and initiate the second DMA cycle. When the 15th bit of the ID cyclic check word is shifted into the Write Buffer, the same thing occurs and another DMA cycle is initiated to transfer this information to the 3rd location in the three-word block in Memory. At the end of the ICCC field, the RG flip-flop is reset and the DS field is entered. RI being true disables the 8-input NAND gate in the DC Counter load 3 logic to prevent presetting the counter to three if a successful ID compare was not made while reading the identifier information.

Upon entering the DS field, 18 bytes are loaded into the B/B Counter as is done during Read Data operations. This is not the full length of the DS field, which is 32 bytes long. The Field Counter is allowed to increment (L6801) to DATA when SYNDET goes true with WFWD, DS, and the B/B Counter equal to zero (all ones). The Read Gate is turned on, as in a normal Read Data operation, to guarantee sync between the recorded fields and the apparent fields as indicated by the Field Counter. The operation continues through the DATA, DCCC, and GB fields without transferring data to Memory. No comparison is made between recorded and generated cyclic check words during the DCCC field.

At the end of the GB field (as defined by the Field Counter), the DC Counter is incremented to DC5. In the DC Counter reset logic, the DC500 signal goes true and produces the DCCL signal if the DMA word count is zero (CNT=0). This resets the DC Counter to DC0. DCCL also causes CONRS to set, which resets CMBSY. The operation is then terminated and the controller goes idle. If the DMA word count is not zero (CNT=0-) the DC Counter will be set to DC3 as in normal Read Data and the controller proceeds with the reading of "headers".

3.7 READ VERIFY OPERATION

Read Verify operates in exactly the same manner as Read Data, except DMA cycles are not initiated to transfer the data to Memory. A brief description of the operation follows.

The operation is initiated by the four-word Disk Control block. As the first sector is encountered, the identifier is read and compared in the normal manner during sector search. If a successful I.D. compare does not occur (SIDCOM=0), the ID cyclic check word is not verified.

Assuming a positive comparison is not made in the first sector encountered, the sector search operation simply continues in the normal manner until the specified sector is identified. The ID cyclic check word is then verified and an error at this time would cause termination at the end of the sector (DC5 time). The operation then progresses to the Data field. When in the Data field, the DMA word count is decremented by one for each word received to determine the length of the operation. RV and CNT=0 in the DMA Word Counter clock logic produce WFRVN0 which with JKCLK1, DATA, and 0EVEN decrement the DMA Word Counter as the 15th bit of each word is being shifted into the Write Buffer. The word count is thus decremented by one for each data word even though DMA cycles do not occur.

While in the Data field, the cyclic check word is recalculated by the CCW Register in the normal manner. When in the DCCC field, the contents of the CCW Register are compared to the cyclic check word read from the disk. If the two do not compare, the Data Cyclic Check Word Error (DACCE) flip-flop is set, causing termination of the operation at the end of the sector (DC5 time). Assuming no error, the operation terminates at the end of the sector if the word count has been decremented to zero, or continues (DC3) to the next sector to verify its ID and Data cyclic check words if the word count does not equal zero.

3.8 SEEK CYLINDER ONLY OPERATION

Seek Cylinder Only is initiated by the four-word Disk Control block. When the contents of the Disk Command Register are decoded, the SEEK signal goes true. The operation is the same as the seek cylinder portion of the Write Data operation, except that this operation terminates immediately after the disk drive has accepted the cylinder address and initiated the seek operation.

During DC1 the cylinder address is sent to the selected disk drive which sends an acknowledge (ADACK) back to the controller when it has accepted and initiated the seek operation. (Acknowledgement of cylinder address receipt applies to Diablo disk drives only. For other disk drives, ADACK- is grounded on rear-edge connector J11 to simulate acknowledgement.) ADACK causes the ADAK1 flip-flop to set on the next clock pulse. ADAK1, DC1, and 00 produce DCS3 which enables the DC Counter to be incremented to DC2 on the next clock pulse. When the B/B Counter goes to zero, DC2, 00, and SEEK produce DCCL which resets the counter to DC0. DCCL also causes the CONRS flip-flop to set which resets the CMBSY flip-flop. The operation is terminated and the controller goes idle. As explained previously, this does not necessarily mean the heads are now located at the specified cylinder. Seek Cylinder Only merely initiates the seek operation. When the seek operation is complete, an associated flip-flop (SCD0, 1, 2, or 3) is set. The status of the flip-flops is determined by inputting status, or by using Sense commands. The sense response output (SER-) is disabled until the controller goes idle if SCD0, 1, 2, or 3 is selected by the Sense Mux during a Seek Cylinder Only (SEEK) operation.

3.9 WRITE FORMAT OPERATION

Write Format is similar in many respects to the Write Data operation. Therefore, the similarities will be described in general and only the differences will be described in detail. A thorough understanding of the Write Data operation is essential to proper understand of the Write Format operation.

Write Format is initiated by the four-word Disk Control block. The information contained in the control block is loaded into the appropriate registers. The Sector Register is normally loaded with zeros to apply an address of zero to the first sector following the Index mark. The word count, which equals the number of sectors to be formatted times the number of words per sector, is loaded into the DMA Word Counter. The DMA Address Register is loaded with the contents of the fourth word in the Disk Control block, but is of no significance since no data transfers will occur during the Write Format operation. Everything recorded during the operation will originate from within the disk controller. The contents of the Disk Command Register are decoded to produce the WF signal which provides overall control of the operation.

At the end of the Disk Control block phase of the operation, SF goes true allowing the DC Counter to increment to DC1. The occurrence of DEXEC during WF and DC0 causes the Sector Register to be cleared to guarantee the first sector number written will be sector zero. During DC1, the cylinder address is sent to the selected disk drive. When the drive has accepted the address and initiated the seek operation, it sends an acknowledgement back to the controller which causes the ADAK1 flip-flop to set. The DC Counter is then incremented to DC2. In DC2, the controller waits for seek complete from the disk drive to indicate the heads are over the addressed cylinder. When the seek complete is received, the SEKCOM signal goes true and the DC Counter is incremented to DC3. In DC3, the controller awaits the generation of an Index pulse. Sector pulses may be generated before an Index pulse, but they will cause no action until after the Index pulse which indicates the start of Sector 0. When the Index pulse is developed (on first Sector pulse after reception of an Index "mark"), the IDX1 flip-flop is set. IDX1, WF, and IDX3- in the increment logic of the DC Counter produce the DCS1 signal. DCS1 enables the DC Counter to be incremented to DC4, the Field Counter to be incremented to IG, and the B/B Counter to be loaded with 40 bytes which is the length of the IG field. LD5 and LD7 are produced in the B/B Counter Loading logic to enable the appropriate preset signals to load the 40 bytes. (Refer to B/B Counter Loading Format table 3-1.) Also as a result of the IDX1 flip-flop, the Write Gate (WG) flip-flop is set to enable writing to commence at the selected disk drive. (Refer to Read, Write, and Erase Gate timing diagram figure 3-11.) With the Field Counter equal to IG, the D1 input to the Write Data Multiplexer is enabled. The D1 input is low at this time so "0"s are written in the IG field for the first 39 of the 40 bytes. (The data is sent to the disk in the double-frequency data/clock stream format as previously described.) At the 40th byte, the D1 input goes high and "1"s are written for the next 7 bit times. During the last bit time in the field, 00 goes true and a "0" is written as the final bit. The : 7F sync character is thus recorded to indicate the beginning of the CY field. In the increment logic of the Field Counter, 00, IG, and WF enable the L6801 signal which causes the Field Counter to be incremented to CY and the B/B Counter to be loaded with two bytes.

When in the CY field, the clock logic for the Cylinder, Head, and Sector Registers is enabled and these registers begin to rotate so their contents can be recorded in the CY and TS fields on the disk. (The CY and TS fields combined are known as the Identifier or Identifier field of the sector.) The CF00 output of the Cylinder Register is applied to the Adder for addition to the Carry flip-flop output. Since the Carry flip-flop is inactive at this time, the Adder output, SUM01, is unchanged SUM01 is applied to the D2 and D3 inputs of the Write Data Multiplexer. With the Field Counter equal to CY, the D2 input is enabled and the contents of the Cylinder Register are thus sent to the disk and recorded in the CY field. At the end of the CY field, the L6801 signal again goes true to enable the Field Counter to be incremented to TS, and the B/B Counter to be loaded with 2 bytes.

While in the TS field, the Cylinder, Head, and Sector Registers continue to be rotated. The contents of the Head and Sector Registers, via the SUM01 signal, are applied through the D3 input of the Write Data Multiplexer and sent to the disk for recording in the TS field. At the end of the TS field, the contents of the Cylinder, Head and Sector Registers are back in their original positions and the identifier is recorded in the CY and TS fields of the sector. The L6801 signal again goes true to enable the Field Counter to be incremented to ICCC and the B/B Counter to be loaded with 2 bytes.

While recording the identifier, the ID cyclic check word is developed in the CCW Register from the data sent to the disk. (Cyclic check word is developed in the same manner as the Data cyclic check word previously described in the Write Data description.) The LSB of the CCW Register, CCW00, is applied to the D4 input of the Write Data Multiplexer, which is enabled during the ICCC field. During the ICCC field, the cyclic check word is shifted out of the register and through the multiplexer to be sent to the disk for recording in the ICCC field. Also during the ICCC field, the Sector ID Compare (SIDCOM) flip-flop is set. Since the RG signal is false, the J input to the SIDC1-flip-flop is disabled. The SIDC1- flip-flop thus remained reset (SIDC1=1) during the CY and TS fields. On the first clock pulse in the ICCC field, the SIDCOM flip-flop is set. SIDCOM is required later for incrementing the Sector or Head address in multiple sector or multiple head operation, respectively.

The D5 input to the Write Data Mulitplexer is the same as the D1 input. The information recorded in the DS field is thus all "0"s, except for the last byte which is a sync character (: 7F). In the increment logic of the Field Counter, DS and WFWD produce L6801 when 00 goes true at the end of the field. On the next clock pulse, the Field Counter is incremented to DATA and, assuming a Data field of 256 words, the B/B Counter is loaded with 512 bytes.

When in the Data field, the D6 input to the Write Data Multiplexer is enabled. The LSB of the Read Buffer (RB00) is applied to the D6 input. The Read Buffer contain all "0"s because "0"s have been shifted into the buffer via its serial input at the MSB (RB15) which is grounded. The S/L input to the buffer is high during Write

Format operation, and the clock input, which is WF and JKCLK2, has been enabled since the Write Format command was decoded. Zeros are therefore shifted into the buffer for the entire operation. During the Data field, the "0"s are shifted out of the Read buffer and sent to the disk for recording. ("0"s are actually the lack of data pulses in the data/clock stream output. Refer to Data/Clock Stream Format (timing diagram figure 3-15).

WF, DATA, 0EVEN, and JKCLK1 decrements the DMA Word Counter (if CNT=0-), at the end of the 15th bit time associated with each 16 bit word of "0"s recorded on the disk in the Data field. The word counter is thus decremented by one for each word recorded in the Data field. At the end of the Data field, the L6801 signal is again produced to enable the Field Counter to be incremented to DCCC and the B/B Counter to be loaded with 2 bytes. While in the DCCC field, the D7 input to the Write Data Muliplexer is enabled. The D7 input is fed from the LSB of the CCW Register, CCW00, as was the D4 input during the ICCC field. The contents of the CCW Register, the Data cyclic check word, are thus recorded in the DCCC field. The cyclic check word will be all "0"s since only "0"s were recorded in the Data field. At the end of the DCCC field, the Field Counter is incremented to GB and the B/B Counter is loaded with 8 bytes. Zeros are recorded in the Guard Byte field since the D0 input to the Write Data Multiplexer is enabled and it is grounded.

At the end of the GB field, 00, DC4, and GB produce GBDC4 which enables the DC Counter to be incremented to DC5 and GB, WFWD, and 00 reset the WG flip-flop, both on the next clock pulse. Assuming more than one sector is to be formatted, the word count would not have been decremented to zero when the Data field was being written with zeros. In this case, DC500, DCCL-, and CNT=0- produce DCCLD which enables the DC Counter to be preset to DC3 on the next clock pulse and the Field Counter to be reset to its quiescent (QUIE) state.

Before the DC Counter is preset to DC3, DC5 and 00 enable the IDX3 flip-flop to set on the next clock pulse as the DC Counter is being preset to DC3. IDX3 being set disables the increment logic of the DC Counter which enabled the counter to be incremented to DC4 upon reception of the first Index pulse (When IDX1 was set at beginning of sector). However, IDX3 and the Sector pulse indicating the start of Sector 1 allows the DC Counter to be incremented to DC4. The WG flip-flop is set by WF, SECTB, IDX3, and DC4 on the next JKCLK. The operation then proceeds as previously described until the TS field is processed when the last bit of the Head (TR) Register is being recorded in the identifier to Sector 1, TS, 01, SIDCOM and SECCOM cause the CARRY flip-flop to set on the next clock pulse. The contents of the Sector Register are incremented by one, and the proper sector address is recorded in the TS field of Sector 1. The remainder of the operation for Sector 1, and subsequent sectors, is exactly the same as previously described for Sector 0.

If more than 12 sectors are to be formatted, the Sector Register is reset to zero at the end of Sector 11. This is done by the TRS signal going true in the reset logic of the Sector Register. On the trailing edge of TRS, the Head Select Register is incremented to enable the next, higher numbered, head at the selected disk drive. The Head (TR) Register is incremented when the TS field associated with Sector 0 of the newly enabled head is processed. CY, 00, SECCOM, and SIDCOM enable the Carry flip-flop to set on the next clock pulse when the LSB of the Head (TR) Register is to be processed. The contents of the Head Register are incremented, and the proper head address is recorded on the disk. (A complete description of the events occurring during Sector 11 and Sector 0 is provided in paragraph 3.3.8 and 3.3.9 respectively, of the Write Data description.)

At the end of the sector in which the word count is decremented to zero, DC500 and CNT=0 enable the DCCL signal which resets the DC Counter to DC0. DCCL causes the CONRS flip-flop to set, which resets the CMBSY flip-flop. The operation is terminated and the disk controller goes idle.

3.10 NOOP

The NOOP command is initiated by the four-word Disk Control block. The information contained in the block is transferred to the disk controller in the normal manner, and is stored in the appropriate registers. The disk controller does not go busy during the command, and the operation is terminated during the fourth DMA cycle when the fourth word of the Disk Control block is extracted from Memory. The Timeout Counter is started as in all other DMA operations.

The contents of the Disk Command Register during the NOOP command will be all zeros. Term NOOP inhibits F3CLK to the CMBSY flip-flop during the third DMA cycle, keeping the CMBSY flip-flop from setting and the disk controller idle. NOOP, FAA4, and STB resets the DMA Initialization Sequencer at the end of the fourth DMA cycle which terminates the operation.

3.11 RESTORE OPERATION (SEL :F,4)

The Restore operation is not initiated by the four-word Disk Control block as are the other operations previously described. Restore is initiated by a Select command having a device address of :F and function code of 4. As the device address is decoded, the ADDR signal goes true. PLSE during the Select command and ADDR in the I/O Command Decode logic produce the APLS signal. APLS, EXEC (true during Select command), and a function code of 4 (AFB00-, AFB01-, AB02) sets the Serial Input latch whose output is ANDed with ADKT4- (presently high) and applied to the serial input of the ring counter. On the leading edge of the next

SRCLK pulse, T1 goes true. (Refer to Restore Operation, timing diagram figure 3-19.) T1 enables the restore (RESTE) signal which is sent to the disk drive to initiate the Restore operation when the strobe goes true. On the trailing edge of the next clock pulse, T2 goes true generating the strobe (SEKPL-) signal which strobes in the RESTE signal at the disk drive and intiates the operation and the leading edge of the next SRCLK pulse sets the Restore Busy (RSBSY) flip-flop which enables the CBUSY signal indicating the controller is busy.

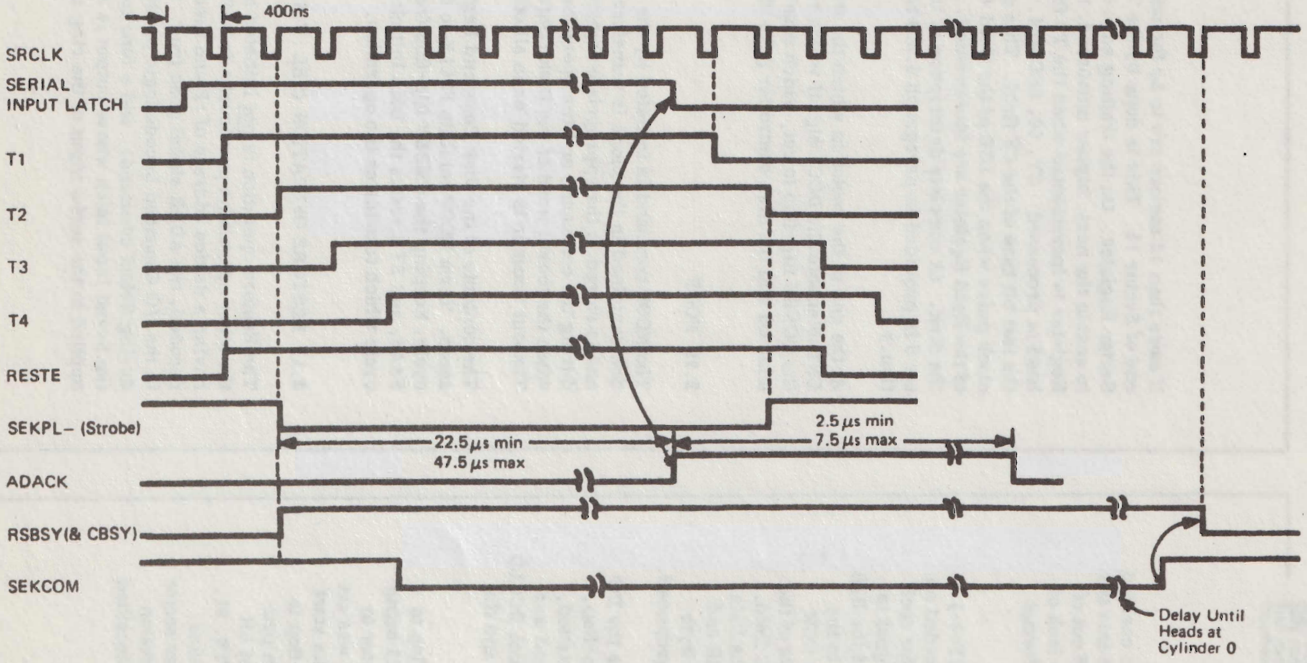


Figure 3-19. Restore Operation, Timing Diagram

As soon as the operation is initiated at the disk drive, the seek complete (SCOM) signal from the drive goes false, causing the SEKCOM signal to also go false. On the next clock pulse, T3 goes true, and on the following pulse, T4 goes true. Conditions remain stable at this time until the disk drive returns an address acknowledge (ADACK) signal which indicates the drive has accepted the RESTE signal and initiated the operation (heads begin to move toward Cylinder 0). ADACK goes true somewhere between 22.5 and 47.5 μs after receipt of the strobe signal. ADACK and T4 reset the Serial Input latch. On the next four clock pulses, T1, T2, T3, and T4 successively go false. When T2 goes false, the SEKPL- signal goes false; and when T3 goes false, the RESTE signal goes false. The acknowledge signal from the drive stays true for a minimum of 2.5 μs, to a maximum of 7.5 μs.

The heads continue to move toward Cylinder 0. When they arrive at Cylinder 0, the SCOM from the drive goes true, causing the SEKCOM signal to also to true. SEKCOM and RESTE cause the RSBSY flip-flop to reset on the next clock pulse. RSBSY going false causes CBUSY to go false and the operation is terminated and the controller goes idle.

3.12 INTERRUPTS

The disk controller is capable of initiating one interrupt each time interrupts are enabled at the controller. This interrupt may be "stimulated" by Process Halt or Seek Complete. (Refer to paragraph 2-16.)

Interrupts are enabled by issuing an Output command with a device address of :F and a function code of 3 (EMASK). EMASK, OUT (true during Output command), and APLS clock the Interrupt Mask (IMSK) flip-flop. The flip-flop is set on the trailing edge of the APLS pulse, enabling one interrupt from the disk controller when the INTS flip-flop sets.

The Process Halt interrupt is initiated by the Process Halt (PHALT) flip-flop being set. PHALT is set after the CONRS flip-flop is set upon termination of any operation initiated by the Disk Control block.

The Seek Complete interrupt is initiated when the seek operation at any on-line disk drive is completed, and the controller is idle. A seek complete (SCD0 thru SCD3) status store flip-flop is associated with each disk drive. Upon completion of a seek (or restore) operation at any of the disk drives, the associated seek complete flip-flop is set. Any one of the four seek complete flip-flops being set and CBUSY- will enable the Interrupt Pending (INTS) flip-flop.

If either of the interrupt initiating events occurs, the INTS flip-flop is set on the next IOCL pulse received from the Processor. INTS and IMSK in the Interrupt Request logic (assuming interrupts are enabled) cause the ME signal to go true to enable the interrupt request (IUR- signal) if the controller has interrupt priority (PRIN true). The interrupt request is sent to the Processor and the controller then awaits an acknowledgement from the Processor in the form of an interrupt address request (IAR- signal true). The ME- signal going true inhibits priority from being passed on to down-stream devices.

Upon reception of the address request, IAR, PRIN, and ME produce the CIAR signal. CIAR enables the D bus drivers associated with the Interrupt Address Encoder. Assuming the standard interrupt address, the E2- and E8- signals are grounded on rear-edge connector J11 of the 531 board. This causes DB01- and DB03- to go true to form the interrupt address of :00A. The Processor then executes the instruction at the interrupt location.

The CIAR signal enables the Interrupt Mask Reset (IMRS) flip-flop to be set on the trailing edge of PLSE. IMRS direct resets the IMSK flip-flop to disable further interrupts until IMSK is once again set. IMSK going false causes ME- to go false (high) which enables interrupt priority (PROT- signal true) to be passed on to down-stream devices. The IMRS flip-flop is then reset upon execution of the next Output command.

The interrupt routine initiated by the interrupt normally contains an Input Status command to determine the cause of the interrupt. Upon completion of the Input command, the status reset (STRST) signal goes true. STRST- being true direct resets the PHALT, and four seek complete flip-flops. The flip-flops are then ready to store further interrupt stimuli as they occur. With all interrupt stimuli thus reset, the D input to the INTS flip-flop goes low, causing the flip-flop to reset on the next IOCL pulse.

3.13 LOGIC NOT PREVIOUSLY DESCRIBED

3.13.1 Read Data/Clock Separator

For certain disk drives other than Diablo, data and clock information is received in the form of a double-frequency read data/clock stream (RDACK0 thru RDACK3). The data and clock information is received via one line and is interspersed (see timing diagram figure 3-20). The data/clock stream inputs from the four possible on-line disk drives are applied to the Read Data/Clock Multiplexer. The output of the multiplexer, RDACLK, is determined by the contents of the Unit Select Register and is associated with the selected disk drive. RDACLK is applied to two gates, one associated with clock pulses and the other with data. The two gates are alternately enabled by the Q and Q- outputs of the Read Data flip-flop (RDFF) which is reset when a clock pulse is imminent, and set when a data pulse is imminent. RDFF is always in the reset state prior to reception of the data/clock stream. This is because the direct reset of the flip-flop remains enabled during that period by the SDATA- signal being false (high) until a data pulse is received. When the Read Gate is enabled in the IG or DS field (see Read Write, and Erase Gate timing diagram figure 3-4), the data/clock stream is received from the selected disk drive. The first pulse to be received will be a clock pulse since only "0"s are recorded in these fields, except for the last byte which is the Sync character (:7F). Since RDFF is reset, the gate associated with clock pulses is enabled and SBCLK- goes true with the first RDACLK pulse. This triggers RDOS which puts out a negative-going pulse of approximately 380ns to remove the reset from RDFF. On the trailing edge of SBCLK-, RDFF is set to disable the gate associated with clock pulses and enable the gate associated with data pulses. No data pulses will be received until the last byte of the IG or DS field. When RDOS times out, which is just beyond the time when data pulses are normally received, RDFF is reset to once again enable the clock associated gate. This cycle is repeated until the data pulses associated with the Sync character are received. The SBCLK- signal continues to go true once each bit-time. SDATA- being true develops the SEPDATA signal, and SBCLK- being true develops the SEPCLK signal. These signals are applied to the Data Recovery logic, previously described under Identifier Sync, paragraph 3.3.6.2.

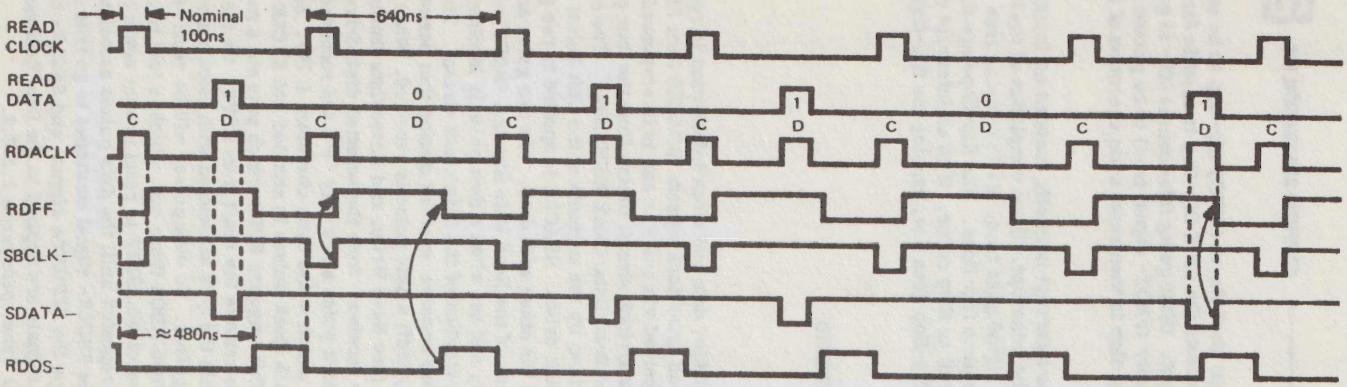


Figure 3-20. Read Data/Clock Separator, Timing Diagram

Occasionally a data pulse may extend beyond the time out period of RDOS (notice last data pulse on timing diagram). In this case, RDFF will not be reset when RDOS times out since SDATA- will still be true, but when SDATA- goes false, RDFF resets.

3.13.2 Timeout Logic (Figure 3-21)

The Timeout logic provides a fixed time period in which disk operations initiated by the controller must be completed. The time period is sufficiently long (minimum of approximately 4.62 seconds) to allow completion of the longest possible operation. The logic is essentially comprised of an oscillator and a counter. The oscillator, comprised of two one-shots, is free-running. The first is triggered when its input goes low (refer to timing diagram digure 3-14). This produces a pulse of approximately 330ms. When it times out, the second one-shot (TMOSQ2) is triggered and it too, produces a 330ms pulse. When it times out, the first is retriggered to keep the oscillator free-running. The trailing edge of TMOSQ2 clocks the Timeout counter, as long as the counter has not reached its error indicating count of eight (TIMEOUT). The counter will not increment, however, until it is enabled by removal of the high from its reset inputs. This occurs when FAA1 goes true at the beginning of a four word Disk Control block transfer. FAA1 direct sets the DACT flip-flop enabling the counter. If a restore operation takes place the RSBUSY flip-flop is set and RSBSY- enables the counter. When the counter is enabled, it will increment to 1 on the first available clock pulse. This can occur just after the operation is initiated, or as much as 660ms (approximate) after initiation because of the asynchronous timing of the FAA1 or RSBSY- signals in relation to the Timeout logic. The counter is then incremented each 660ms thereafter, until it is disabled by:

1. The counter reaching eight (TIMEOUT).
2. The address acknowledgement from the disk drive (RSBUSY flip-flop reseting).
3. The end of the Disk Control block initiated operation (DMRSA resets the DACT flip-flop).

For Disk Control block initiated operations, the longest operation, including worst-case considerations, would be approximately 1.6 seconds. This would be a Write Format operation in which an entire cylinder in a 20-head disk drive is formatted. Worst-case Restore operations are longer (approximately 2.9 seconds), but the Timeout logic is only enabled during initiation of the operation, not until completion.

Should the counter not be disabled by DACT- or RSBSY- going false, the counter would continue to be incremented each 660ms until it reached a count of eight (approximately between 4.62 and 5.28 seconds after being enabled). At that time, the TIMEOUT signal goes true. TIMEOUT being true disables further clocking pulses to the counter, and also ensures the counter will not be reset when DEXEC- or RESTE- goes false. The counter acts as an error flag and will remain stable until status is input to the Processor to determine the cause of the failure. TIMEOUT or DRDY- produce Drive Not Ready Or Timeout (DNRTIM). DNRTIM is applied to the reset logic of the Disk Control Counter where it causes the counter to be reset to DC0, thus terminating the stalled operation. DNRTIM- is applied to the Sense Multiplexer to make the error condition available to the Processor through use of Sense commands. TIMEOUT is applied to the D bus Multiplexer and Drivers (associated with status and DMA word count) to make the error condition available through Status input. When status is input, STRST- will go true to reset the Timeout Counter to zero. TIMEOUT- then goes false to allow clocking pulses to be applied to the counter, and also to keep the counter disabled until the next operation is initiated.

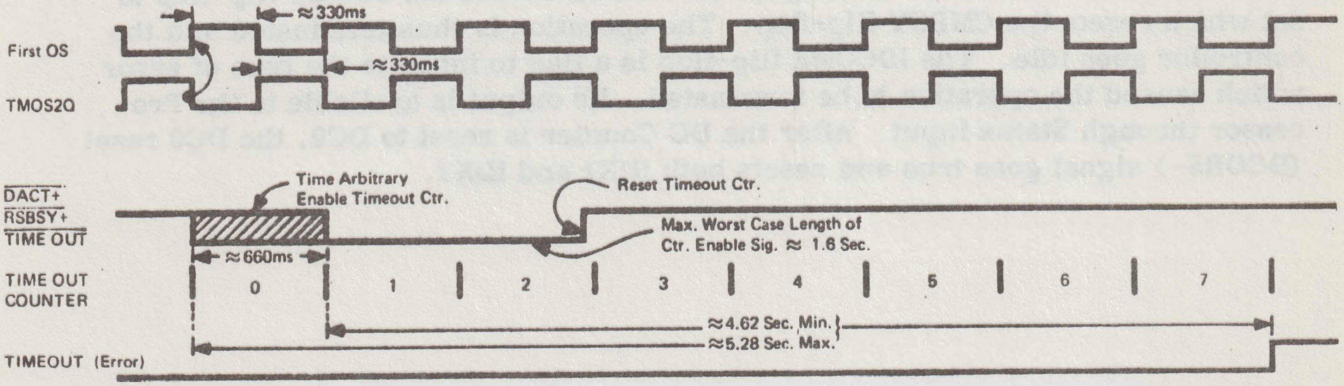

≈330ms
First OS
≈330ms
TMOS2Q
Time Arbitrary Enable Timeout Ctr.
Reset Timeout Ctr.
$\overline{\text{DACT+}}$
$\overline{\text{RSBSY+}}$
$\overline{\text{TIME OUT}}$
Max. Worst Case Length of Ctr. Enable Sig. ≈ 1.6 Sec.
≈660ms
TIME OUT COUNTER
0
1
2
3
4
5
6
7
≈4.62 Sec. Min.
≈5.28 Sec. Max.
TIMEOUT (Error)

Figure 3-21. Timeout Logic

3.13.3 No ID Compare (Figure 3-22)

Logic is employed by the disk controller to detect and store the error condition indicating a positive ID compare was not made within at least one full revolution of the disk. This logic includes the Index Pulse Register flip-flops IDX1 and IDX2, and the ID Search Error flip-flop, IDCOME.

When an operation is initiated by the four-word Disk Control block, the heads are moved to the addressed cylinder, the appropriate head is enabled, and the DC Counter is incremented to DC3 to await the first Index or Sector pulse to start the sector search operation. Assuming only a Sector pulse is developed at the beginning of the next sector, the normal sequence of events occur whereby the DC Counter is incremented to DC4 and an ID comparison is made. (Refer to Identifier Comparison, paragraph 3.3.6.4.) Further assuming no comparison, the SIDC1- flip-flop is set and the SIDC1 signal goes false to prevent SIDCOM from setting in the ICCC field (see timing diagram figure 3-15). With SIDCOM- high, the DC Counter reverts back to DC3 to await the next Sector pulse. The sector search operation then continues through succeeding sectors in exactly the same manner as previously described. When the Index pulse is developed at the beginning of Sector 0, the IDX1 flip-flop is set on the next clock pulse (the same one which increments the DC Counter to DC4). On the next clock pulse, IDX2 is set and IDX1 is reset. IDX2 acts as a reference to indicate the Index pulse has been received at least once for a given track. All sectors associated with that track are then searched for a positive ID compare. If sectors were searched prior to the Index pulse, those sectors will be searched again. When the Index pulse is developed for the second time, IDX1 again goes true and with IDX2, DC4, and SIDCOM- produces 2IDX which causes the IDCOME flip-flop to set and resets the DC Counter to DC0 by enabling DCCL. DCCL causes the CONRS flip-flop to set which resets the CMBSY flip-flop. The operation is thus terminated and the controller goes idle. The IDCOME flip-flop is a flag to indicate the type of error which caused the operation to be terminated. Its output is available to the Processor through Status input. After the DC Counter is reset to DC0, the DC0 reset (DCORS-) signal goes true and resets both IDX1 and IDX2.

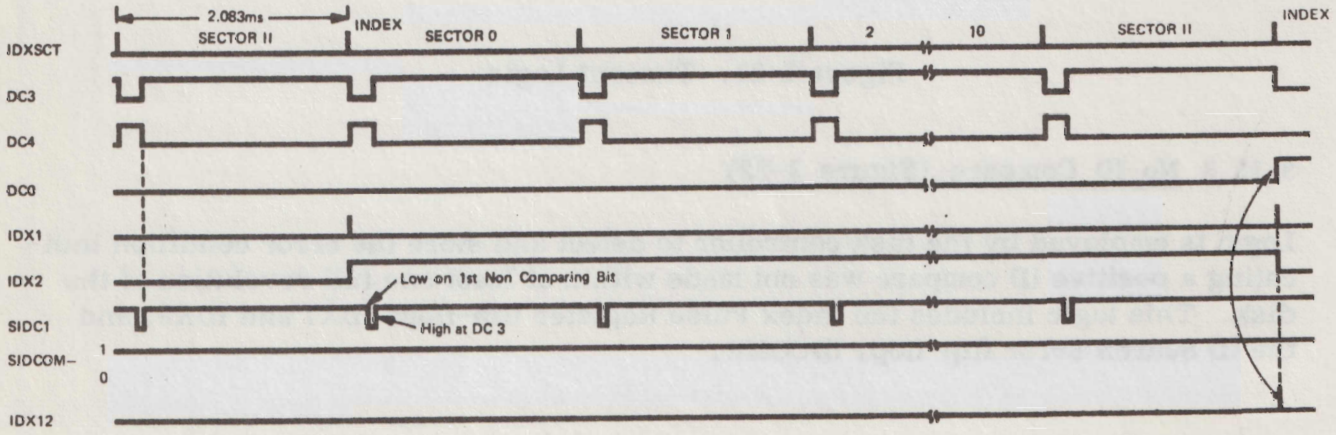


Figure 3-22. No ID Compare, Timing Diagram

3.13.4 Write Gate and Sector/Index Mark Overlap

In operations other than Write Format, the write gate should not be on when an index pulse (INDEX) or sector pulse (SECTB) is encountered. If this does occur, the Write Gate flip-flop is cleared, the Disk Control and Field Counters are reset, and the operation is aborted.

Appendix A

GLOSSARY OF MNEMONICS

A.1 GENERAL

This appendix lists the Moving Head Disk controller mnemonics and their meanings.

A.2 I/O BUS SIGNAL DEFINITIONS

The Moving Head Disk controller does not communicate directly with the Processor. It uses logic lines which are common to all peripheral interfaces. Table A-1 defines the common logic signals used by the Moving Head Disk controller.

A.3 MOVING HEAD DISK CONTROLLER SIGNAL DEFINITIONS

Signals associated with the Moving Head Disk controller or the disk drive(s) connected to it are defined in table A-2.

Table A-1. I/O Bus Signal Definitions

MNEMONIC	DESCRIPTION
AB00-thru AB15-	Address (A) Bus Lines 0-15. Sixteen lines which are time shared by the Processor and DMA controllers. Fifteen of the A bus lines (0-14) are used to address memory locations. The 16th line (bit 15, the MSB) is used to specify word or byte memory operation. During I/O operations, the Processor uses the low order 8-bits of the A bus to convey device address and function code information to I/O devices. The high order 8-bits contain random information and are not normally used. The format of the low order 8-bits during I/O operations, and a description of each field follows:

AB07-	Device Address bit 4	
AB06-	Device Address bit 3	
AB05-	Device Address bit 2	P Field
AB04-	Device Address bit 1	
AB03-	Device Address bit 0	
AB02-	Function Code bit 2	
AB01-	Function Code bit 1	F Field
AB00-	Function Code bit 0	

Table A-2. Moving Head Disk. Signal Definitions (Cont.)

	1. Function (F) Field Lines. Three common lines which carry the function code to all I/O interface controllers during execution of an I/O command. Only the particular controller enabled by the device address (contained on P field lines at same time) will be able to utilize the function code. 2. Peripheral (P) Field Lines. Five common lines which carry the device address to all I/O interface controllers during execution of an I/O command. The device address will enable the particular controller which has been previously assigned a similar device address.
DB00-thru DB15-	Data D Bus Line 0-15. Sixteen common bidirectional lines whic are time shared by the Processor, Memory, and I/O interface controllers. The Processor uses the D bus to transfer data to and from memory. It also uses the D bus to transfer data to and from the I/O interface controllers. DMA controllers use the D bus to transfer data to and from memory. I/O interface controllers use the D bus to convey the interrupt address to the Processor during interrupt processing.
DPIN-	DMA Priority In. Priority string input for direct memory access. When True, indicates no device having higher DMA priority has access to Memory, and that this controller may gain access to memory if it so desires. This is done by issuing a "stop processor" request (STOP- signal true) to gain control of the I/O bus.
DPOT-	DMA Priority Out. Priority string output for direct memory access. When true, indicates no device having higher DMA priority, nor this device, has access to memory, and that DMA priority is being passed on to down-stream devices.
EXEC-	Execute. Processor generated signal which indicates the I/O command being executed by the Processor is a Select or Select and Present command. EXEC- is typically used to set or reset controls in the addressed interface controller.

Table A-2. Moving Head Disk. Signal Definitions (Cont.)

IAR-	Interrupt Address Request. Processor response to interrupt request (IUR-signal) for interrupt address from interrupting device controller at the start of IUA (interrupt acknowledge).
IN-	Input Processor generated signal which indicates the I/O command being executed is an Input command and that the addressed interface controller should now place the data to be transferred to the Processor on the Data bus.
INA-	Input. Refer to IN-.
IOCL-	I/O Clock. Processor generated 2.5 MHz pulse train having a minimum pulse width of 150 ns. The signal is used by I/O interface controllers to synchronize IUR interrupts into the Processor. IOCL is inhibited during IUA (interrupt acknowledge) and slows down to 1.25 MHz during I/O transfer time.
IUR-	Interrupt Request. Common interrupt request line to Processor which can be used by any device interface controller. This line will initiate the interrupt, but the interrupt address must be supplied by the interrupting controller during IAR time. If two or more interface controller's request interrupt service at the same time, recognition is given to the controller having the highest priority via the interrupt priority string (PRIN- and PROT-).
MACK-	Memory Acknowledge. Memory generated signal which informs the Processor or DMA controller which has access to Memory that data is available during a read operation, or that data has been stored during a write operation.
MDIS-	Memory Disable. Signal from power supply which, when true, indicates power is failing. Disables DMA logic in controller.
MRD-	Read Mode. Refer to RD-.
MST-	Memory Start. Processor or DMA controller generated signal which initiates a memory cycle.
OUT-	Output. Processor generated signal which indicates the I/O command being executed is an Output command. It also indicates the Processor has placed the data to be transferred on the Data bus and the addressed interface controller should accept it.

Table A-2. Moving Head Disk. Signal Definitions (Cont.)

PFD-	Power Fail Detect. Signal generated by power supply whenever ac input power falls below a predetermined threshold. The signal forces DMA operations to terminate in order to permit an orderly shut down of the system by the Processor.
PLSE-	Pulse. Negative-going pulse between 100 and 250 ns in duration, which is active during the latter half of the EXEC, IN, OUT and IAR signals. Used as a clock or strobe by the addressed I/O interface controller.
PRIN-	Priority In. Priority string input for program interrupts, when true, indicates that neither IL1, IL2, PF/R nor any other up-stream (higher priority) I/O interface controller is requesting an interrupt, and that this controller may request an interrupt.
PROT-	Priority Out. Priority string output for program interrupts when true, indicates that no up-stream I/O interface controller, nor this controller, is requesting an interrupt and that priority is being passed on to down-stream controllers.
RD-	Read Mode Processor or DMA controller generated signal which, when low, indicates the current memory cycle is a read/restore cycle. When high RD- indicates the current memory cycle is a clear/write cycle.
RST-	System Reset. Processor or Console generated signal which is used to reset all controls in ALL I/O interface controllers to a known starting configuration. RST- is generated by the Processor in response to a power failure conditon, an Autoload initiation sequence, or when the Console RESET switch is depressed.
RSXT-	System Reset. Refer to RST-.
SACK-	Stop Acknowledge. Processor generated signal indicating the Processor has relinquished control of the I/O bus to the DMA controller which requested memory access (generated STOP-signal). If more than one controller requested memory access, the one having DMA priority will gain control of the I/O bus.
SER-	Sense Response. When true, indicates a true response to an interrogation by the Processor (through the use of a Sense or

Table A-2. Moving Head Disk. Signal Definitions (Cont.)

	conditional I/O command) of some function associated with the addressed I/O interface controller, or the device it controls.
SPRIN-	Priority In. Refer to PRIN-.
SPROT-	Priority Out. Refer to PROT-.
STOP-	Stop Processor. DMA controller generated signal which stops the Processor upon completion of its current machine cycle to permit the DMA controller to gain control of the I/O bus. STOP- may be generated at any time and may remain active for any length of time.
TYP1-	Type 1 Processor Installed. This signal is ground-true when the LSI-1 Processor is installed and open when the LSI-2 Processor is installed. This signal permits DMA controllers to determine which processor is installed and perform hog mode transfers if necessary.

Table A-2. Moving Head Disk. Signal Definitions

MNEMONIC	LOC	DESCRIPTION
00,01 70,71	530- A,B,25	Bit/Byte Counter Decode. Decoded outputs of Bit/Byte counter during last two "byte times" before end-of-count (when counter equals all "1"s). The LSB indicates the byte, and the MSB indicates the bit. Since the counter is loaded with the 1's complement of the number of bits to be counted, and the counter counts up, the smaller the byte number (and bit number within the byte), the closer to the end of the count. Refer to the chart below for decode definitions.

	BYTE 1	BYTE 0
BITS	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0

MNEMONIC	LOC	DESCRIPTION
015	530- C25	Bit/Byte Counter Decode. Byte 15, Bit 0.
0EVEN	530- B26	Bit/Byte Counter Decode. Indicates 15 bits of a 16 bit word have been written on or read from the disk.

Table A-2. Moving Head Disk. Signal Definitions (Cont.)

2COY1-	530- B34	Byte Counter Decode. Indicates bits YC04, YC03, and YC02 are all equal to "1".
2IDX	530- B19	Two Index. Indicates the controller has sensed two index marks while unsuccessfully searching for a specific Identifier field (cylinder-head-sector address and flag bits).
2SECCL	531- C42	2 Sector Marks Clock. Clock input to SECDV flip-flop when two Sector marks received for each sector. Strapped on rear-edge connector J11 to SECTX signal.
4,10,20 STRAP-	531- A36	Number of heads select. Static input signals from rear-edge connector J11. When an input is grounded, it indicates the number of heads being used on the disk drive (4,10, or 20 respectively).
ADACK	531- B43	Address Acknowledge. Buffered input signal from Diablo disk drive only, indicating the drive has accepted the cylinder address sent to it.
ADAK1	530- D20	Address Acknowledge, DC1. Output of flip-flop which stores address acknowledge from Diablo disk drive in disk control count one (DC1) time.
ADDR	531- A11	Address. Indicates that bits 3 thru 7 of the A Bus compare to the "device address" of the disk controller as strapped on rear edge connector J11.
AFB00-thru AFB02-	531- B11	A Bus bits 0-2. Buffered inputs from function section of A Bus.
AINZX-	531- C9	Initialize. Function code 3, EXEC, PLSE, and the device address (ADDR) from the processor causes the controller to be set to a known state.
APLS	531- C11	Address and Pulse. Combination of ADDR and PLSE signals.
ASCOM0,1 2, 3,	531- A,B,27	Seek Complete 0, 1, 2, 3, (polarity corrected). Same as corresponding SCOM signal, except polarity corrected to ensure positive-true signal. (See SCPOL.)

Table A-2. Moving Head Disk. Signal Definitions (Cont.)

BC01 thru BC03	530- A26	Bit Counter 01-03. Output signals from Bit counter portion of Bit/Byte counter which counts the bits in each byte. (BC01 is LSB and BC03 is MSB.)
BIT0,2, 6, 7	530- B25	Bit Counter Decode 0, 2, 6, 7. Decoded outputs (1's complement) of Bit counter. BIT0 is true when BC01, 02, and 03 equal all "1"s. BIT7 is true when BC01, 02, and 03 equal all "0"s.
BUS0-thru BUS7-	531- C,D46	Bus Lines 0-7. Bus lines to disk drive which carry output of Output Bus Multiplexer. Output of multiplexer contains cylinder address during DC1, track address during DC2, and status information when RESTE signal goes true.
BYTE0, 1,2	530- A25	Byte Counter Decode 0, 1,2, Decode of Byte counter outputs YC01 thru YC08. BYTE 0, 1, and 2 indicates the last byte, next to last byte, or 2nd from last byte, respectively, is being processed.
CAE-	531- C47	Cylinder Address Extend. Used as MSB of cylinder address on disk drives containing 406 or 408 cylinders.
CARRY	530- B31	Output of the CARRY flip-flop which performs binary serial addition to the contents of the Head Sector Registers as they are rotated. This is done only after a previous sector identification has occurred.
CBSYRS	531- A10	Command Busy Reset. Signal produced by CONRS or RST signals which resets the CMBSY and RH flip-flops, and clears the DMA Initialization Sequencer.
CBUSY	531- A9	Controller Busy. Indicates controller is busy performing a command as output from Memory via DMA, or a head restore operation in the selected disk drive.
CCW00	530- D35	Cyclic Check Word 00-. Output signal of Cyclic Check Words Register. CCW00 is check bit for all "1" bits written in bit 0 position.
CF	530- C12	Clock Frequency. Output of oscillator (OSC) divided by 2 and synchronized with the Read Clock.
CF00 thru CF15	530- A,B, C,D30	Cylinder Register 00-15. Output signals from cylinder register. CF15 is MSB and CF00 is LSB.

Table A-2. Moving Head Disk. Signal Definitions (Cont.)

CIAR-	531- B13	Controller Interrupt Address Request. Goes true when Processor responds to interrupt request with an interrupt address request (IAR) if the controller has interrupt priority. CIAR gates the interrupt address onto the Data bus lines, and allows the Interrupt Mask Reset (IMRS) flip-flop to set when PLSE occurs.
CLKDATA	531- A37	Clocked Data. Output of CLKDATA flip-flop. Flip-flop delays and temporarily stores the stabilized data pulse (Output of JITDATA flip-flop) for insertion into the RDATA flip-flop. All received data is delayed by one bit-time.
CMBSY	531- A10	Command Busy. Indicates controller is busy performing a command.
CNT = 0	531- C31	Counter = 0. Goes true when DMA Counter has been decremented to zero.
COBC	530- A26	Carry Out of Bit Counter. Goes true when Bit Counter (BC01 thru BC03) and LSB of Byte Counter (YC00) are all equal to "1".
CONRS	531- B10	Controller Reset. Output of the CONRS flip-flop which is set when the Disk Control Counter is cleared during the DMA execute (DEXEC) state of the DMA State Counter. CONRS causes the Process Halt (PHALT) flip-flop to set and direct resets the CMBSY flip-flop.
COY1,2	530- B26, C26	Carry Out of Byte Counter 1,2. Carry out signals from Byte Counter. COY1 indicates YC01 thru YC04 equals all "1"s, and COY2 indicates YC05 thru YC08 equals all "1"s.
CRCEN-	531- B10	Cyclic Check Word Register Connection Enable. Gates the contents of the Cyclic Check Word Register onto the Data bus lines for transfer to the Processor when an input command with a function code of 2 is executed by the disk controller.
CY	530- A23	Cylinder Field. Output of Field Count decoder which indicates the head is over the Cylinder field of a sector.
D0 thru D3	531- B,C26	Drive 0-3. Decodes of Unit Select flip-flops which indicate disk drive selected by bits 0 and 1 of word 2 of the 4 word Disk Control block.

Table A-2. Moving Head Disk. Signal Definitions (Cont.)

DA1, DA2	531- C27	Drive Address 1,2. Outputs of Unit Select Register which stores the number of the selected disk drive as contained in word 2 of the Disk Control block.
DACCE	531- B31	Data Cyclic Check Word Error. Output of DACCE flip-flop. Indicates cyclic check word error occurred while reading Data field, signifying a bit(s) was dropped or picked up. Prerecorded cyclic check word is compared to cyclic check word generated while reading Data field to determine presence of error.
DACT	531- B34	DMA Active. Output of DACT flip-flop which is set when the Initialization Sequencer goes to FAA1. It is cleared by the DMA Request Reset (DMRSA) signal.
DATA	530- B23	Data Field. Output of Field Count Decoder indicating head is over Data field of a sector. The Data field holds a maximum of 512 bytes (256 words) of data.
DC0 thru DC5	530- A,B17	Disk Count 0-5. Output signals from Disk Count Decoder which indicates contents of Disk Control Counter. The significance of each count follows. DC1. Seek operation started (move head to addressed cylinder). DC2. Complete seek operation. DC3. Find initial starting point on selected track to start operation. DC4. Read or write data or identifier information. DC5. Provides recycle (reset to DC3) or end-of-operation (reset to DC0) control.
DC0RS 1,2	530- C17	General (DC0) Reset, Combination of JKCLK and DC0 or System Reset (RSXT-).
DC500	530- A20	DC5 and 00. Indicates Disk Control Counter has been incremented to DC5 and Bit-Byte counter zero (all "1"s), signifying end-of-sector.
DCCC	530- B23	Data Cyclic Check Word. Output signal from Field Count Decoder indicating head is over Data Cyclic Check Word field of a sector.

Table A-2. Moving Head Disk. Signal Definitions (Cont.)

DCCL	530- B18	Disk Control Counter Clear. Signal used to clear Disk Control Counter. Signal is initiated by various conditions existing which warrant the clearing of the counter and termination of the present operation.
DCCL1	530- A19	Disk Control Counter Clear One. Generates DCCL when conditions occur during DC5 and Bit/Byte time 00 which require the resetting of the Disk Control Counter.
DCCL2	530- B19	Disk Control Counter Clear Two. Generates DCCL when an unsafe condition (UNSAFE) occurs at a disk drive, an Index or Sector mark is encountered during a write operation, or at the end of DC2 (Bit/Byte Counter = 00) if performing a Seek Only operation.
DCCL3	530- B19	Disk Control Counter Clear Three. Generates DCCL wh a seek error (SEEKER) occurs, the selected disk drive i not ready (DRDY), or if the operation has exceeded the time limit (TIMEOUT).
DCCLD-	530- A18	Disk Control Counter Load. Signal used to parallel load the Disk Control Counter. The counter is loaded with 3 (DC3) when the signal is true and the clock input goes high.
DCLD1-	530- A18	Disk Control Counter Load One. Generates DCCLD- at the end of DC5 if no errors have occurred and the word count is not equal to zero.
DCLD2-	530- A18	Disk Control Counter Load Two. Generates DCCLD- if no sector identification occurs.
DCLK	531- D39	Diablo Read Clock. Read clock line from Diablo disk drive. Diablo provides separate Read Clock and Read Data lines instead of double frequency data-clock strea
DCS1,2,3	530- C19,D18	Disk Control Counter Strobe 1, 2, 3. Three of four signals which enable the Disk Control counter to be incremented.
DDATA	531- B39	Diablo Read Data. Data input (buffered) from Diablo disk drives. (See DCLK.)

Table A-2. Moving Head Disk. Signal Definitions (Cont.)

DEN2-	531- D23	Data Enable 2. Signal produced during DC4 time which enables the contents of the Read Buffer (RB) to be placed on the Data bus for transfer to Memory.
DEXEC	531- A23	DMA Execute. Final state of DMA Initialization Sequencer. Indicates all four words of Disk Control block have been extracted from Memory, and command to be executed is other than a NOOP. When the sequencer reaches this state, control of the disk controller is assumed by the Disk Control Counter.
DI00 thru DI15	531- A,B,C, D30	Data Input 00-15 (to Processor). Output signals from Data Bus Multiplexer. Output of multiplexer is contents of DMA Word Counter, or status information.
DMARQA	530- A33	DMA Request. Request for DMA cycle with DMA word count not equal to zero. The signal is used in the DMA Request logic to initiate a DMA cycle.
DMARS-	531- B18	DMA Request Reset. Clears the flip-flops associated with a DMA Request.
DMRQA	530- B33	DMA Request. See DMARQA.
DMRSA-	531- B24	DMA Reset. Resets the Initialization Sequencer and DACT flip-flop at the end of FAA4 if in a NOOP condition or when the controller goes idle (CBSYRS).
DNRTIM	531- D43	Drive Not Ready or Timeout. When true, indicates selected disk drive is not ready (see DRDY), or operation being performed exceeded maximum allowable time period (see TIMEOUT). DNRTIM going true resets the Disk Control Counter.
DOUT	531- C10	Device Address and Output. Combination of OUT, ADDR, and CBUSY- signals, indicating Output command is to be executed by disk controller if controller is not already busy.
DRDY	530- C42	Drive Ready. Indicates the selected disk drive is ready to operate. DRDY generally signifies the following (may vary slightly with type of disk drive): 1. Power applied. 2. Disk cartridge loaded. 3. Door closed.

Table A-2. Moving Head Disk. Signal Definitions (Cont.)

		4. LOAD/RUN switch in RUN position. 5. Disk rotating at proper RPM. 6. No UNSAFE condition exists.
DRIDD-	530- B33	DMA Read or ID Request, Delayed. Output of DRIDD flip-flop which delays DMA requests initiated by Read Data (RDDRQ) or Read ID (RIDRQ) by one bit time. If delay were not incorporated, DMA cycle would occur one bit time early since RDDRQ and RIDRQ are enabled by the 0EVEN signal which goes true after 15 bits of a 16 bit word have been read.
DS	530- B23	Data Sync. Output of Field Count Decoder indicating head is over Data Sync field of a sector. During Write Data (and Write Format) operation, "0"s are written for the first 31 of 32 bytes in the field. A : 7F is written as the last byte. The DS field synchronizes the controller with reception of the zeros during a Read operation in preparation for reading the Data field.
DSTART-	531- B18	DMA State Sequencer Start. Allows the DMA State Sequencer to advance if the controller has priority (DPIN) and a stop acknowledge (SACK) is present. It is generated when the RQ and START flip-flops are both set.
DV2Q-	531- C41	Sector Divide. Output of flip-flop which causes the Sector marks received from the selected disk to be divided by two. This provides the 12 sector divisions for disks which output 24 Sector marks per revolution.
E2-,E4- E32-,E64-, E128-,E256-	531- A,B14	Enable 2,4,8,16,32,64,128,256. Eight static input lines from rear-edge connector J11-A6 thru A13 that are applied to the Interrupt Address Encoder. If an input is grounded, the equivalent decimal value is added to the interrupt address sent to the Processor. For example, if E8- is grounded, 8_{10} is added to the interrupt address. The "standard" interrupt address for the Moving Head Disk controller is :0A (10_{10}). This requires E8- and E2- to be grounded.
ECA	530- A14	Enable Cylinder Address. Enables contents of Cylinder (CY) Register (CF15 - CF8) to be applied to the Output bus (OTB0 thru OTBS7) for transfer to the selected disk

Table A-2. Moving Head Disk. Signal Definitions (Cont.)

		drive by producing the SELA signal. Also enables bit 7 (CF7) of the CY register to be transferred to the disk drive if a 406 cylinder drive is used. Bit 7, in this case, would be the MSB of the address.
EOC	531-A32	End-of-Cylinder. Indicates DMA Word Counter had not been decremented to zero (words still remain to be written, read, formatted, etc.) when the disk operation had been performed in the last available sector of the addressed cylinder. TR register = last available head and SE register = maximum sector count (normally 11). Read, Write, or other disk operations are normally performed starting at the addressed head and sector in the addressed cylinder, and working down the cylinder by incrementing the head address and using the 12 sectors associated with each head in the cylinder, until the DMA Word Counter has been decremented to zero.
EMASK	531-C11	Enable Mask. Goes true when an Output command with the appropriate device address and a function code of 3 is executed, to enable clocking of the IMSK flip-flop.
EQ3	531-B17	Extended Q3. Q3 signal of the DMA State Sequencer with the negative transition delayed.
ERGT	531-A46	Erase Gate. Output signal to disk drive(s). Same as WRGT.
F1CLK F2CLK F3CLK	531-A23	Field 1, 2, and 3 Clock. Outputs of DMA Initialization Sequencer (ANDed with STB) which go true when the first, second, and third words, respectively, of the four word Disk Control block are extracted from Memory. The functions of each follows: F1CLK. Clocks sector address and head address into Sector and Head (TR) Registers respectively. Clocks the RS1 flip-flop for detection of a difference in platter being used on a four head drive. F2CLK. Clocks cylinder address into Cylinder Register and unit select bits into Unit Select flip-flops. Clocks the RS2 flip-flop for detection of a difference in disk drive numbers from the one used previously.

Table A-2. Moving Head Disk. Signal Definitions (Cont.)

		F3CLK. Clocks word count into DMA Word Counter. Clocks the CMBSY and RH flip-flops when going false.
FAA1 thru FAA3	531-A22	DMA Initialization Sequencer 1-3. Outputs from DMA Initialization Sequencer which enable the F1CLK, F2CLK, and F3CLK.
FAA4	531-A22	DMA Initialization Sequencer 4. During this time examination is made for a NOOP condition. The DMA Address Register is loaded if not in a NOOP.
FC00 thru FC03	530-A,B23	Field Counter 00-03. FC00 is the LSB and FC03 is the MS of the Field Counter which keeps track of head location (field within a sector over which head is located). The Field Counter outputs are decoded by the Field Count Decoder.
FCLK	531-B19	A free running 10 MHz clock used primarily for generating SCLK to increment the DMA State Sequencer.
FQDX	531-B23	This signal indicates that the Initialization Sequencer is active and in a state other than FAA4. It allows the incrementation of the DMA Address Register at the end of each state (except FAA4) of the Initialization Sequencer.
FREQ	531-A19	Control Field DMA Request. Logical ORing of FAA1, FAA2, and FAA3 outputs of DMA State sequencer which forces DMA requests for succeeding words in Disk control block.
GB	530-B23	Guard Bytes Field. Output signal from Field Count Decoder indicating head is over GB field of a sector. Eight guard bytes are written in the GB field.
GBDC4	530-C19	Guard Bytes, DC4 and Bit/Byte Counter = all "1"s. Combination of GB, DC4, and 00 signals which enables incrementing the Disk Control Counter to DC5 when the last bit of the eight guard bytes has been written or read
HAERF	531-B35	Head Address Error Flip-Flop. Indicates the contents of the Head (TR) Register exceeds the maximum numbered head available which is head 1 for 2 head disk drive, head 3 for 4 head disk drive, etc. This F/F is set only at SF time thus if for some reason an erroneous head number occurs during data transfers this F/F will not be set In the latter case a No ID Compare Status should occur.

Table A-2. Moving Head Disk. Signal Definitions (Cont.)

HAERR	531- B35	Head Address Error. Output of Head Address comparator which compares the contents of the Head (TR) Register to the static strapped inputs (4, 10, or 20 STRAP) indicates the maximum numbered head. Two results are possible. During times when the SF signal is false, the TR00 bit is considered for comparison as the LSB. In this case, HAERR will go true if TR00 thru TR04 is equal to, or greater than the maximum numbered head. The signal is used for "last sector in cylinder" comparison. (See LS00.) When SF is true (for one bit time just after the four control words are extracted from Memory) the TR00 bit is disregarded for comparison. In this case, if the contents of the TR Register are greater than the maximum numbered head, HAERR will go true and cause the HAERF flip-flop to set.
HEADTG-	531- C47	Strobe Head Address. Output signal to disk drive(s). Same as SHA.
SEL0,1	530- A,B29	Head Select 0,1. Output signals from Head Select Register which contains addressed head number (0 thru 3 only). The Head Select Register is used with disk drives containing a maximum of four heads. HSEL1 is the MSB and HSEL0 is the LSB. Register is loaded when SF flip-flop is set.
ICCC	530- A23	Identifier Cyclic Check Word. Output of Field Count Decoder which indicates head is over Identifier Cyclic Check Word field of a sector. Even parity is recorded in field for bits contained in CY and TS fields.
IDCCE	531- A31	Identifier Cyclic Check Word Error. Output of IDCCE flip-flop which is set when the Identifier cyclic check word read from the disk does not compare with the contents of the Cyclic Check Word Register after the Identifier (CY and TS) field has been read.
IDCOME	531- A32	Identifier Compare Error. Indicates addressed sector could not be found before reception of two Index marks. Identifier information read from ID fields of the 12 sectors associated with a particular cylinder and head, could not be found to match the contents of the Cylinder, Head (TR) and Sector Registers.

Table A-2. Moving Head Disk. Signal Definitions (Cont.)

IDX1	530- C22	Index 1. Output of IDX1 flip-flop which is set upon reception of Index pulse when in DC3 time. IDX1 is used during Formatting of disk to enable incrementing of Disk Control Counter when certain other conditions are present. Also used in conjunction with IDX2 to indicate an Identifier Search error if reception of 2nd Index pulse occurs without a sector compare.
IDX2	530- D22	Index 2. Output of IDX2 flip-flop which is set on next JKCLK2 clock pulse after IDX1 is set. (IDX1 is reset on this clock pulse.) IDX2 and IDX1 indicate an Identifier Search error if the contents of the Cylinder, TR (head) and Sector Registers did not match the contents of the Identifier field in one of the 12 sectors being searched.
IDX3	530- C20	Index 3. Output of IDX3 flip-flop which is set when the Disk Control Counter is incremented to DC5 for the first time after an operation is started, indicating at least one sector was processed.
IDXFF	531- B41	Index Flip-Flop. Output of IDXFF flip-flop which stores the occurrence of an Index mark. Flip-flop is reset upon reception of the next Sector pulse (Output of SECTB flip-flop).
IG	530- A23	Identifier Gap. Output of Field Count Decoder which indicates the head is over the Identifier Gap of a sector. This includes the 24-byte Sector Gap field and the 16-byte Identifier Sync field. The Sector Gap field allows for jitter, write amplifier recovery, mechanical alignment, and other problems before reading from the disk. The Identifier Sync field syncs the controller receive circuitry for reading the Identifier field. Written as 15 bytes of "0"s and 1 byte of : 7F.
IMRS	531- C14	Interrupt Mask Reset. Output of IMRS flip-flop which is set when the interrupt address is gated onto the Data bus for transfer to the Processor. IMRS direct resets the IMSK flip-flop.
IMSK	531- C14	Interrupt Mask. Output of IMSK flip-flop, when set, enables interrupts from the disk controller.

Table A-2. Moving Head Disk. Signal Definitions (Cont.)

INADR	531- B11	Input and Device Address. Combination of IN and ADDR signals which indicates an Input command is being executed by the disk controller.
INDEX	531- B41	Index Pulse. Output of IDXFF and Sector pulse (SECTB) indicate the Index point (start of Sector 0) on the disk platter(s). Referred to as Index pulse.
INDXB	531- B42	Index Mark B. Raw Index mark from disk drive. Occurs shortly after Sector mark in center of Sector 11, if "standard" of 12 sectors is used with 24 Sector disk pack.
INTS	531- C15	Interrupt Store. Output of INTS flip-flop which, when true, initiates an interrupt if the IMSK flip-flop is set and priority (PRIN-signal) is available to the disk controller.
INZX	531- D9	Initialize. Initialize signal in sync with the controller JKCLK. (Refer to AINZX-.)
JITDATA	531- A38	Jitter Data. Output of JITDATA flip-flop. Flip-flop stabilizes (de-jitters) incoming data pulses.
JKCLK1, 2,3	530- C11	J-K Flip-Flop Clock 1,2,3. Clock pulses used for clocking most of the J-K type flip-flops in the controller. Source of the clock pulses is the oscillator when performing all functions except Read. During Read operations, the source for the clock is the RCLK pulses. RCLK is either separated from the Read Data and Clock (RDACLK) input stream, or, if the Diablo disk drive is being used, the DCLK input from that disk drive.
JMP	530- D28	Jumper. Signal source for JMP2 thru JMP5 signals which determines number of bytes to be written in, or read from the Data field of all sectors. The signal originates on the 530 board during DS time, is wired to the 531 board through the interboard cable, and applied to pin A28 of P11. From there it is jumpered to the appropriate JMP2 thru 5 input pin, if required.

Table A-2. Moving Head Disk. Signal Definitions (Cont.)

JMP2 thru JMP5	531- B,C15	Jumper 2-5. Static input signals originating on conne tor J11 of 531 board which determine count to be prelo ed into Byte Counter for Data field. (Determines num of bytes in Data field of each sector.) The appropriat input pin is strapped to the JMP- signal (531 board, J A28), which is the signal source. The signals are wi to the 530 board via the Bit/Byte counter loading logic The number of bytes per Data field as determined by these jumpers is listed in the chart below:

BYTES IN DATA FIELD	SIG. STRAPPED TO JMP-
512	N/C
480	JMP2-
448	JMP3-
416	JMP2-, JMP3-
384	JMP4-
352	JMP2-, JMP4-
320	JMP3-, JMP4-
288	JMP2-, JMP3-, JMP4-
256	JMP5-
224	JMP2-, JMP5-
192	JMP3-, JMP5-
160	JMP2, JMP3, JMP5-
128	JMP4-, JMP5-
96	JMP2-, JMP4-, JMP5-
64	JMP3-, JMP4-, JMP5-
32	JMP2-, JMP3-, JMP4-, J

KRSBSY	531- C33	K input to the RSBSY flip-flop. Allows the RSBSY fli flop to reset when the seek operation is complete (SEKCOM) during a restore operation (RESTE).
L2WDS	530- C25	Last 2 Words. Decode of Bit/Byte Counter output wh indicates two words (four bytes) remain to be writte or read in any field.
L6801	530- C23	Increment Field Counter. Allows the Field Counter t advance at the end of a field (00). Enables the prelo ing of the Bit/Byte Counter.
LCMD	531- C10	Load Command. Signal developed when an Output c mand with the appropriate device address and a fun code other than 3 is executed by the controller. LC loads the DMA Address Register with the contents of Data bus, which contains the beginning address of t

Table A-2. Moving Head Disk. Signal Definitions (Cont.)

		four-word Disk Control block in Memory. The signal parallel loads the DMA Initialization Sequencer to FAA1 which indicates the first word of the control field is being extracted from Memory.
LD1 thru LD8	530-B,C,D27 A,B,C,D28	Load 1-8. Signals originating in Bit/Byte Counter Loading logic which enable various counts to be preloaded into the Bit/Byte Counter for the various fields of a sector. The signals go true in the "previous" field so the appropriate count for the following field may be loaded at the end of the "previous" field.
LS00-	530-B20	Last Sector in Cylinder. Indicates processing of final sector in a given cylinder (Maximum numbered sector associated with maximum numbered head) is complete, and DMA word count is still not equal to zero. Signal causes Disk Control Counter to be reset at end of maximum numbered sector (DC5 and Bit/Byte counter equal to all "1"s), and the EOC flip-flop to be set.
LSIHG	531-B15	LSI 1 Hog. Forces the controller into the Hog mode by allowing the RHFF flip-flop to be directly set if in the DS field during a RD, WD, or RI mode of operation.
LYC00 thru LYC08	530-A,B,C,D27	Load Byte X. Parallel load signals to the Byte Counter. LYC00 = LSB and LYC08 = MSB.
ME	531-B13	Interrupt, Logical AND of INTS and IMSK. Initiates an interrupt if priority (PRIN- true) is available to the controller.
MIN1 thru MIN4	531-A,B,C,D30	Minimum 1,2,3,4. Output signals from four 4-bit counters which comprise the DMA Word Counter. When true, the signals indicate their respective 4-bit counter equals zero (one's complement).
NOOP	531-A15	No Operation. Output from the Disk Command Decoder indicating no operation is to take place in relation to the last command issued.
OSC	530-A11	Oscillator. Crystal-controlled oscillator output used for clock generation in all functions except Read. The frequency of the oscillator, depends upon the type of disk drive used with the controller.

Table A-2. Moving Head Disk. Signal Definitions (Cont.)

OTBS0 thru OTBS7	530-A,B,C,D13	Output Bus 0-7. Output signals from the Output Bus Multiplexer which are sent to the disk drive(s). The Output bus carries cylinder address, head (TR) address, and control information to the selected disk drive.
PHALT-	531-C16	Process Halt. Output of PHALT (interrupt stimulus store) flip-flop which causes the Interrupt Store (INTS) flip-flop to set, when true. PHALT is set when the present operation is being terminated (Disk Control Counter being cleared to DC0).
PS0 thru PS4	531-A12	Peripheral Select 0-4. Static input signals from rear-edge connector J11-A1 thru A5 which are used to assign the "device address" of the disk controller. The "standard" device address of the disk controller is : 0F which requires A1 thru A4 to be grounded.
Q1 thru Q3	531-C17,18	DMA State Sequencer 1-3. Output signals from DMA State Sequencer which indicates the present control state of the DMA logic. The DMA State Sequencer is stepped for each DMA memory cycle performed.
QUIE	530-A23	Quiescent. When true, indicates the Field Counter is in the quiescent state (all zeros).
RATDIS	531-C18	Rate Disable. The output of the RATDIS flip-flop allow the DMA State Sequencer to cycle out if a rate error (RATER) occurs or if the DMA active (DACT) flip-flop is reset before the end of a DMA state sequence.
RATER	531-D19	Rate Error. Output of RATER flip-flop which is set when a second DMA request is being made by the controller, but the Processor has not yet responded to the first with a DMA acknowledge.
RB00 thru RB15	530-A,B,C,D37	Read Buffer 00-15. Output signals from the Read Buffer. During a Write operation, data is transferred in parallel from the Write Buffer (WB) register to the Read Buffer (RB) register and shifted out serially from the RB00 position to be written. During Read operations, Read data is shifted into the WB register serially (WB15 position to WB00 position) and then transferred in

Table A-2. Moving Head Disk. Signal Definitions (Cont.)

		parallel to the RB register for temporary storage before transfer to Memory. Data contained in the RB register during Write operations is in a positive-true form ("1" = +5 Vdc). During Read operations, it is in a negative-true form ("1" = 0 Vdc).
RCB	531- C38	Read Clock B. Output pulse from RCB one-shot which is adjusted to time-out approximately 120 ns after the trailing edge of the RCLK pulse. The RDATA flip-flop is clocked by the trailing edge of RCB-.
RCLK	531- C38	Read Clock. Output pulse of approximately 62 ns from RCLK one-shot. One-shot is triggered on leading edge of SEPCLK pulse. Clock pulses for disk controller (JKCLK and SRCLK) are developed from RCLK pulses during periods of data reception.
RCLK1,2	530- B11	Read Clock 1,2. Outputs from RCLK1 and RCLK2 flip-flops which synchronize the transition from the internally generated clock source (OSC) to the externally generated clock source from the selected disk drive (RCLK) when going into a Read operation, and vice-versa when coming out of a Read operation. This ensures that no clock spikes will occur, and the period between adjacent clock pulses (JKCLK1, etc.) will never be less than the normal bit time.
RD	531- B15	Read Data or Read Data (Hog Mode). Logical OR of RE and RH signals which are outputs from the Command decoder indicating Read Data or Read Data (Hog Mode) respectively.
RD⊕CCC-	531- A31	Read Data EX ORed with Cyclic Check Word. Output of EX OR gate (ANDed with Read Gate) which serially compares the contents of the recorded cyclic check word (Identifier or Data) with the contents of the Cyclic Check Word Register. If the signal goes high, an error has occurred and IDCCE is set.
RDACK0 thru RDACK3-	531- A,B40	Read Data/Read Clock Stream 0-3. Read Data and Read Clock stream input from disk drives 0 thru 3.

Table A-2. Moving Head Disk. Signal Definitions (Cont.)

RDACLK	531- B39	Read Data/Read Clock Stream. Read Data and Read Clo stream input from selected disk drive. (Multiplexed ou put of RDACK0 thru RDACK3.) This one line contains both Read Data and Read Clock information. The inform tion is separated by the Read Data Separator logic. (No used with Diablo disk drives which transmit data and clock information separately.)
RDATA-	531- A37	Read Data. Output of the RDATA flip-flop which is a stretched and delayed version of the Read Data receivec from the disk drive. The received data is stabilized an delayed by the JITDATA and CLKDATA flip-flops, and then stretched (temporarily stored in RDATA flip-flop) so as to be available for clocking into the Write Buffer.
RDDRQ	530- A34	Read Data DMA Request. DMA cycle request made during Read Data or Read Data (Hog Mode) operation. RDDRQ goes true one bit time early when only 15 bits of a word have been read. Signal is then delayed one bit time by DRIDD flip-flop (to allow time for the 16th bit to be clocked into the Write Buffer) before being sent to DMA Control logic on 531 board.
RDFF	531- C39	Read Data Flip-Flop. Set on trailing edge of SCLK puls to enable separation of data from double-frequency Re Data/Read Clock stream (RDACLK). Reset after time slot in which data is contained on data/clock stream. When reset, enables separation of clock pulses from da clock stream.
RDGT	531- B46	Read Gate. Read Gate signal to selected disk drive whi enables its Read Clock and Read Data output line(s). Same as RGA signal.
RDOS	531- C40	Read Data One-Shot. Triggered on leading edge of SCLK- pulse to produce a pulse of approximately 480 ns (when bit-time is 640 ns). RDOS direct resets the RDF when it times out. This is normally after the time when data can be received on the Read Data/Read Clock strea (Resetting of RDFF can be delayed slightly if "1" is received and SDATA-signal is still true after RDOS times out.)

Table A-2. Moving Head Disk. Signal Definitions (Cont.)

RESTE	531- C33	Restore. Signal sent to the selected disk drive to restore the heads to Cylinder 0. Signal also enables the C3 input to the Output Bus Multiplexer for transfer of Read Gate, Write Gate, Erase Gate, and Restore information to the disk via the Output bus if it does not have separate input lines to accommodate these control signals.
REQ	531- A18	DMA Request. Output of the REQ flip-flop which is direct set by RHFF or RQ to initiate a DMA request and generate a stop request (STOP).
RG, RGA	530- A9	Read Gate. Output of RG flip-flop which enables the Read Data and Read Clock line(s) in the selected disk drive.
RGK	530- B10	Read Gate (flip-flop) K input. K input to RG flip-flop which causes the flip-flop to reset when true. (True when Bit/Byte Counter equals all "1"s at end of Identifier or Data Cyclic Check Word field during Read operation.) The signal is also applied to the K input to the RCLK1 flip-flop, causing it to toggle to the reset state on the next RCLK pulse.
RH-	531- A15	Read (Hog Mode). Output of Command Decoder indicating a Read Data operation in the "hog" mode which gives the disk controller exclusive control of Memory. In this case, STOP- is held true (low) to continuously request DMA cycles.
RHFF	531- B19	Read (Hog Mode) Flip-Flop. Set when RH signal goes true to keep STOP- signal true to continuously request DMA cycles until all data has been transferred, or end of cylinder is reached.
RI	531- A15	Read Identifier. Output of Command Decoder which indicates a Read Identifier operation is being performed.
RIDRQ	530- A34	Read Identifier DMA Request. DMA cycle request made during Read Identifier operation. RIDRQ goes true one bit time early when only 15 bits of a word from the Identifier field has been read. Signal is then delayed one bit (to be clocked into the Write Buffer)before being sent to DMA Control logic on the 531 board.

Table A-2. Moving Head Disk. Signal Definitions (Cont.)

RQ	531- A18	DMA Request. Output of the RQ flip-flop which is the initial flip-flop set in an ordinary DMA request (not Hog Mode).
RS1-	531- B43	Resync 1. Output of RS1 flip-flop (RS1 signal high) if the head address contained in the first word of the Control block being extracted from Memory indicates a change of platter (4-head, 2-platter disk drives only). This will allow the controller to resync to the new Index and Sector marks which will now be originating from the other platter. Heads 0 and 1 are associated with the first platter, and heads 2 and 3 with the second platter.
RS2	531- A43	Resync 2. Output of RS2 flip-flop which is set when the disk drive address contained in the second word of the Disk Control block being extracted from Memory indicates a different drive from the one used previously. This will allow the controller to resync to the new source of Index and Sector marks.
RS12-	531- A43	Resync 1 or 2. Logical ORing of RS1 and RS2 signals. RS12-going low sets the SYNRS flip-flop.
RSBSY	531- B10	Restore Busy. Output of RSBSY flip-flop which is set when a Restore operation is taking place at the selected disk drive. This restores the heads to Cylinder 0. RSBSY enables the CBUSY signal.
RV-	531- A15	Read Verify. Output from Command Decoder indicating a Read Verify operation is taking place.
RWDQ	530- B34	Request Write Data. Signal which initiates DMA request for data during Write operation. This occurs under two different conditions: 1. When 2 bytes are left to be read in Data Sync field which allows sufficient time to access the data, clock it into the Write Buffer, and then transfer it to the Read Buffer.

Table A-2. Moving Head Disk. Signal Definitions (Cont.)

		2. After 15 bits of each word have been written in the Data field until only two words are left to be written. (At that time, the Write Buffer and Read Buffer each contain a word, which are the last two words to be written.) The RWDQ signal enables the DMRQA signal if WD and SIDCOM are true.
SBCLK	531- C39	Raw clock as it is initially seperated from the data-clock stream from the disk drive.
SCA	530- B21	Strobe Cylinder Address. Output of SCA flip-flop which is set at DC1 when Bit/Byte Counter decode 70 is true. (Bit/Byte Counter is loaded with this count at same time Disk Control Counter is incremented from 0 to 1.) The output of the flip-flop is sent to the selected disk drive to strobe in the cylinder address. The cylinder address is placed on the Output bus by enabling the C3 inputs to the Output Bus Multiplexer (DC1 and Byte 0).
SCD0,1,2,3	531- A,B,C, D25	Seek Complete Drive 0,1,2,3. Outputs from SCD0,1,2, and 3 flip-flops which store cylinder seek completed signal from disk drives 0,1,2, and 3 respectively.
SCLK	531- B18	Sequencer Clock. Controlled FCLK used to increment the DMA State Sequencer.
SCOMO,1, 2,3	531- A,B,C28	Seek Complete 0,1,2,3. Signals from disk drives 0,1, 2 and 3 respectively, indicating completion of the seek operation (heads positioned over addressed cylinder).
SCPOL	531- A27	Seek Complete Polarity. Static input signal which controls seek complete signal polarity correction network to ensure proper polarity of these signals for integration into controller logic. If the input signals (SCOMO-SCOM3) are negative-true ("1" = 0 Vdc), SCPOL (pin B5 on J11 of 531 board) should be connected to ground (available on pins B2 and B3 of J11). If the signals are positive-true, SCPOL should be left open.
SCSE0,1, 2,3	531- A,B,C, D25	Seek Complete Status Enable 0,1,2,3. Output of flip-flops associated with disk drives 0,1,2, and 3 which enable the storage of seek complete signals from the associated units. Appropriate enable flip-flop is set when cylinder address is strobed into associated disk drive (T2SCA signal).

Table A-2. Moving Head Disk. Signal Definitions (Cont.)

SDATA-	531- C39	Separated Data. Data information separated from Read Data/Read Clock stream input.
SE00 thru SE07	530- A,B31	Sector Register 0-7. Output signals from the Sector Register which stores the number of the sector being accessed.
SECCOM-	530- C32	Last Sector Complete. Output of SECCOM flip-flop which is set upon completion of maximum numbered sector.
SECM1	531- C34	Last Sector Compare. Indicates contents of Sector Register are equal to maximum sector number as determined by rear-edge connector J11 jumpering scheme. The "standard" maximum number normally assigned is 11 (Sectors 0-11).
SECTB	531- D41	Sector Pulse. Output of SECTB flip-flop which is the Sector pulse used by the controller. Occurs 12 times per revolution of the disk (if "standard" 12 sectors is used).
SECTX	531- D42	Sector Mark. Raw Sector Mark as received from the selected disk drive.
SEEK	531- A15	Seek Cylinder. Output from Disk Command Decoder indicating a Seek addressed cylinder operation is taking place.
SEEKER	531- D43	Seek Error. Signal from selected disk drive indicating an incomplete cylinder seek operation (heads did not get to addressed cylinder). Signal will stay true until a Restore command (SEL F,4) is issued to restore the heads to Cylinder 0.
SEKCOM	531 B27	Seek Complete. Indicates Seek operation at selected disk drive is complete (heads are over addressed cylinder).
SEKPL-	531- B46	Seek Cylinder Pulse. Signal to selected disk drive whic strobes in the cylinder address and initiates a "seek" operation. Signal is initiated by SCA signal, or T2 signal from Restore logic. If initiated by T2, heads will be restored to Cylinder 0.

Table A-2. Moving Head Disk. Signal Definitions (Cont.)

SELECT0,1 2,3	531- A48	Select (Disk Drive) 0,1,2,3. Output signals to disk drives 0,1,2, and 3 which select the respective unit, if true.
SELRS	531- C9	Select Restore. Result from a processor command for a Restore operation. Initiates the Restore Operation.
SEPCLK	531- C38	Separated Clock. Clock pulses: 1. from Read Data/Clock separator when information is received in data/clock stream, or 2. direct from disk drive which employes its own separator.
SEPDATA	531- C38	Separated Data. Data pulses: 1. from Read Data/Clock separator when information is received in data/clock stream, or 2. direct from disk drive which employes its own separator.
SF	530- A21	Sync Flip-Flop. Set when all four words of the Disk Control block have been extracted from Memory. The flip-flop synchronizes transfer of control from the DMA Control logic to the Disk Control Counter. Enables incrementing Disk Control Counter from DC0 to DC1.
SHA	530- C21	Strobe Head Address. Output of SHA flip-flop which strobes the head address into the selected disk drive. (Only on disk drives requiring a strobe.)
SIDC1-	530- D32	Sector ID Compare Not. Output of SIDC1-flip-flop which, when remaining reset at the end of the CY and TS fields, indicates a successful comparison between the CY, TR and SE registers and the identifier information read from the disk sector. The flip-flop is reset at DC3. Comparison is carried out in DC4. If any of the 32 bits associated with the CY and TS fields do not compare to the contents of the associated registers, the SIDC1- flip-flop is set to indicate no comparison. Disk Control Counter is then set back to DC3 to try for another comparison in the next sector.

Table A-2. Moving Head Disk. Signal Definitions (Cont.)

SIDCOM	530- D32	Sector ID Compare. Output of flip-flop which is set at ICCC time if a successful ID comparison was made (SIDC1 flip-flop still reset).
SRCLK1,2	530- C11	Shift Register Clock 1,2. Same as JKCLK1,2,3 clocks, except inverted for device requiring negative-going edge for clocking.
SS00 thru SS04	531- C,D36	Sector Select 00-04. Static input signals from rear-edge connector 531-J11 (A23 thru A27) which are used to assign the number, in binary code, of the highest numbered sector on disk platters (normally 11, which indicates 12 sectors, 0 thru 11). The information is used for "last sector compare", which compares the static input lines to the contents of the Sector Register.
START	531- A17	The output of the Start flip-flop which is set by the Stop Acknowledge signal (SACK) if the REQ flip-flop is set. START inhibits DMA priority (DPOT) from "down stream" devices during a DMA request by the Disk Controller.
STB	531- B23	Strobe occurs at the end of the last state (Q3) of the DMA State Sequencer. It is used to generate the Initialization Sequencer clocks (F1CLK-F3CLK) to perform other DMA strobing functions.
STRST	531- D10	Status Reset. Signal which resets status flip-flops and a counter whenever an input command is executed by the controller, if the controller is not busy. The flip-flops and counter reset by the signal are: PHALT RATER Timeout Counter IDCCE HAERF EOC DACCE IDCOME SCD0 thru SCD3
SUM01	531- A31	Summation 01. Output of Adder which is in the "serial addition loop" of the Sector Head (TR), and CY registers. SUM01 updates the contents of the Head Sector registers as they are rotated (along with CY register) when the head is over the CY and TS field of a sector. The signal is also used for sector ID compare and when performing a Write Format operation in the CY and TS fields.

Table A-2. Moving Head Disk. Signal Definitions (Cont.)

SYNDET	530- A40	Sync Character Detect. Indicates the sync character at the end of the Identifier or Data Sync fields has been detected. The sync character is written as a :7F.
SYNFS	531- A42	Sync Reset Flip-Flop Set. SYNFS direct sets the SYNRS flip-flop. Signal is enabled by RS12- signal going true, or when a multiple head operation is taking place on a 4-head disk drive and the controller is about to switch from Head 1 to Head 2 (Head 2 located on second disk platter). These conditions indicate a new source of Index and Sector marks. Hence the need to set the Sync Reset flip-flop.
SYNRS	531- B41	Sync Reset. Output of SYNRS flip-flop which is set to resynchronize the controller when the source of Index and Sector marks is changed. The signal direct sets the SECDV flip-flop, and direct resets the IDXFF and SECTB flip-flops to prevent any Index or Sector pulses until the Index mark from the new source is received.
T1, T2, T3, T4	531- C33	Twisted-Ring Counter 1,2,3,4. Output signals from twisted-ring counter which provides timing for a Restore operation at the selected disk drive (See RESTE).
T2SCA	531- B47	T2 or Strobe Cylinder Address. Pulse which clocks the "seek complete" status enable flip-flops on its trailing edge. The set flip-flop enables the setting of the corresponding SCDX flip-flop when the seek complete (SCOMX) signal is received from the selected drive.
TIMEOUT	531- A33	Timeout. Output signal from Timeout logic. When true, indicates operation being performed has stalled, thus exceeding the maximum allowable time period for any disk operation. This time period extends to be approximately 4.62 to 5.28 seconds after initiation of the operation.
TMOS2Q	531- A34,35	Timeout One-Shot. Output signal from two-one-shots which comprise the oscillator portion of the Timeout logic.

Table A-2. Moving Head Disk. Signal Definitions (Cont.)

TR00 thru TR07	530- C,D31	Head (TR) Register 00-07. Output signals from Head Register which contains the address of the selected head. TR00 is LSB and TR07 is MSB.
TR0IN	531- C36	TR00- or SF. Logical OR of TR00- and SF signals. TR0IN and TR0IN- are used as LSB inputs to Head Address Comparator. During times when SF is false, the TR00 bit is considered for comparison as the LSB. When SF is true, it disables the TR00 input (See HAERR).
TRS	530- B31	Sector Register Reset. Reset Sector register to zero at end of maximum numbered sector (normally 11). Also indicates, in multiple-head operations, that next higher numbered head is about to be accessed. (Used for Index and Sector mark resync on 531 board if next head is on second platter of 4-head disk drive. See SYNFS.)
TS-	530- A23	Track and Sector Fields. Output of Field Count Decoder indicating head is over Head and Sector field in a sector. Head and sector addresses written here.
UNSAFE	531- B43,44	Unsafe (Write Check). Input from selected disk drive indicating a condition(s) exists which is disabling to Write function. Refer to specific disk drive maintenance manual or product description for conditions indicated by UNSAFE line. The UNSAFE signal resets the Disk Contro Counter to zero (DC0).
WB00 thru WB15	530- A-D38	Write Buffer 00-15. Output signals from Write Buffer.
WC00-thru WC15-	531- A-D30	Word Counter 00-15. Output signals from DMA Word Counter.
WCLKA	531- D31	Word Clock A. Clocks the DMA Word Counter during Write Format operations, or Read Verify operations wher the DMA Word Counter is not equal to zero.
WCLKB	531- D31	Word Clock B. Clocks the DMA Word Counter during DMA cycles when data words are being transferred to or from Memory.

Table A-2. Moving Head Disk. Signal Definitions (Cont.)

WCSTSEN	531-C11	Word Count/Status Enable. Causes the word count or status information to be applied to the D bus in response to a Function Code of 0 (status) or 1 (word count) and an input command from the Processor.
WD	531-A15	Write Data. Output from Command Decoder indicating a Write Data operation is taking place.
WDAC0 thru WDAC3	531-C,D48	Write Data and Clock 0, 1, 2, 3. Double frequency Write Data and Clock stream to Disk Drive 0, 1, 2, 3 respectively.
WDAT	530-D35	Write Data. Double frequency Write Data and Clock stream.
WDMUX	530-D36	Write Data Multiplexer. Output signal from Write Data Multiplexer. Which input is routed to the output is determined by the contents of the Field Counter.
WF-	531-A15	Write Format. Output from Write Command Decoder indicating a Write Format operation is taking place.
WFIDX	530-C19	Write Format Index Mark. Indicates to the Write Gate logic that either the first index mark has occurred. If the first index pulse and sector have been recognized (IDX3=1) WFIDX indicates the occurrence of a sector pulse (SECTB). This applies to Write Format operations only.
WFRVN0	531-D32	Write Format or Read Verify with WC ≠ 0.
WFWD	530-B28	Write Format or Write Data operation.
WG	530-B9	Write Gate. Output of WG flip-flop used primarily to enable the write current on the selected head at the selected disk drive. Also produces the EGA signal.
WGJ	530-B10	Write Gate (flip-flop), J Input. J input to WG flip-flop which causes the flip-flop to set when true. Enabled during WF or WD operations when certain other conditions are met.

Table A-2. Moving Head Disk. Signal Definitions (Cont.)

WGK	530-B10	Write Gate (flip-flop), K Input. K input to WG flip-flop which causes the flip-flop to reset when true. Signal is enabled during Write Data operation at end of Guard Bytes field.
WPTOUT-	531-D46	Write Protect Output. Signal enabled by power fail detect (PFD) signal from power supply which disables write current at selected disk drive. This protects against erroneous recording of data when power is being dropped.
WRGT-	531-B46	Write Gate. Write Gate signal to disk drives (see WG).
WRPTCT	531-C44	Write Protected. Signal from currently selected disk drive indicating it is write protected and will not record any data.
Y1EP, Y2EP	530-B,C26	Byte Counter Enable Pulse 1,2. When true, Y1EP enables counting in YC01 thru YC04 portion of Byte counter. Y2EP enables counting in YC05 thru YC08 portion.
YC00 thru YC08	530-A,B,C D26	Byte Counter 00-08. Nine output signals from Byte counter portion of Bit/Byte Counter. YC00 is LSB of these signals and YC08 is the MSB.

Appendix B

DEVICE ADDRESS AND FUNCTION CODE CONVERSION

B.1 GENERAL

Table B-1 provides the two least significant digits of a hexadecimal I/O instruction code from a known device address and function code. For example, a device address of :E and a function code of 6 would equal :76.

Table B-1. Device Address and Function Code Conversion

DA,FC*	INST CODE	DA,FC*	INST CODE	DA,FC*	INST CODE	DA,FC*	INST CODE
:0,0	:XX00	:4,0	:XX20	:8,0	:XX40	:C,0	:XX60
:0,1	01	:4,1	21	:8,1	41	:C,1	61
:0,2	02	:4,2	22	:8,2	42	:C,2	62
:0,3	03	:4,3	23	:8,3	43	:C,3	63
:0,4	04	:4,4	24	:8,4	44	:C,4	64
:0,5	05	:4,5	25	:8,5	45	:C,5	65
:0,6	06	:4,6	26	:8,6	46	:C,6	66
:0,7	07	:4,7	27	:8,7	47	:C,7	67
:1,0	:XX08	:5,0	:XX28	:9,0	:XX48	:D,0	:XX68
:1,1	09	:5,1	29	:9,1	49	:D,1	69
:1,2	0A	:5,2	2A	:9,2	4A	:D,2	6A
:1,3	0B	:5,3	2B	:9,3	4B	:D,3	6B
:1,4	0C	:5,4	2C	:9,4	4C	:D,4	6C
:1,5	0D	:5,5	2D	:9,5	4D	:D,5	6D
:1,6	0E	:5,6	2E	:9,6	4E	:D,6	6E
:1,7	0F	:5,7	2F	:9,7	4F	:D,7	6F
:2,0	:XX10	:6,0	XX30	:A,0	:XX50	:E,0	:XX70
:2,1	11	:6,1	31	:A,1	51	:E,1	71
:2,2	12	:6,2	32	:A,2	52	:E,2	72
:2,3	13	:6,3	33	:A,3	53	:E,3	73
:2,4	14	:6,4	34	:A,4	54	:E,4	74
:2,5	15	:6,5	35	:A,5	55	:E,5	75
:2,6	16	:6,6	36	:A,6	56	:E,6	76
:2,7	17	:6,7	37	:A,7	57	:E,7	77
:3,0	:XX18	:7,0	:XX38	:B,0	:XX58	:F,0	:XX78
:3,1	19	:7,1	39	:B,1	59	:F,1	79
:3,2	1A	:7,2	3A	:B,2	5A	:F,2	7A
:3,3	1B	:7,3	3B	:B,3	5B	:F,3	7B
:3,4	1C	:7,4	3C	:B,4	5C	:F,4	7C
:3,5	1D	:7,5	3D	:B,5	5D	:F,5	7D
:3,6	1E	:7,6	3E	:B,6	5E	:F,6	7E
:3,7	1F	:7,7	3F	:B,7	5F	:F,7	7F

*DA,FC = Device Address, Function Code

Table B-1. Device Address and Function Code Conversion (Cont'd)

DA,FC*	INST CODE	DA,FC*	INST CODE	DA,FC*	INST CODE	DA,FC*	INST CODE
:10,0	:XX80	:14,0	:XXA0	:18,0	:XXC0	:1C,0	:XXE0
:10,1	81	:14,1	A1	:18,1	C1	:1C,1	E1
:10,2	82	:14,2	A2	:18,2	C2	:1C,2	E2
:10,3	83	:14,3	A3	:18,3	C3	:1C,3	E3
:10,4	84	:14,4	A4	:18,4	C4	:1C,4	E4
:10,5	85	:14,5	A5	:18,5	C5	:1C,5	E5
:10,6	86	:14,6	A6	:18,6	C6	:1C,6	E6
:10,7	87	:14,7	A7	:18,7	C7	:1C,7	E7
:11,0	:XX88	:15,0	:XXA8	:19,0	:XXC8	:1D,0	:XXE8
:11,1	89	:15,1	A9	:19,1	C9	:1D,1	E9
:11,2	8A	:15,2	AA	:19,2	CA	:1D,2	EA
:11,3	8B	:15,3	AB	:19,3	CB	:1D,3	EB
:11,4	8C	:15,4	AC	:19,4	CC	:1D,4	EC
:11,5	8D	:15,5	AD	:19,5	CD	:1D,5	ED
:11,6	8E	:15,6	AE	:19,6	CE	:1D,6	EE
:11,7	8F	:15,7	AF	:19,7	CF	:1D,7	EF
:12,0	:XX90	:16,0	:XXB0	:1A,0	:XXD0	:1E,0	:XXF0
:12,1	91	:16,1	B1	:1A,1	D1	:1E,1	F1
:12,2	92	:16,2	B2	:1A,2	D2	:1E,2	F2
:12,3	93	:16,2	B3	:1A,3	D3	:1E,3	F3
:12,4	94	:16,4	B4	:1A,4	D4	:1E,4	F4
:12,5	95	:16,5	B5	:1A,5	D5	:1E,5	F5
:12,6	96	:16,6	B6	:1A,6	D6	:1E,6	F6
:12,7	97	:16,7	B7	:1A,7	D7	:1E,7	F7
:13,0	:XX98	:17,0	:XXB8	:1B,0	:XXD8	:1F,0	:XXF8
:13,1	99	:17,1	B9	:1B,1	D9	:1F,1	F9
:13,2	9A	:17,2	BA	:1B,2	DA	:1F,2	FA
:13,3	9B	:17,3	BB	:1B,3	DB	:1F,3	FB
:13,4	9C	:17,4	BC	:1B,4	DC	:1F,4	FC
:13,5	9D	:17,5	BD	:1B,5	DD	:1F,5	FD
:13,6	9E	:17,6	BE	:1B,6	DE	:1F,6	FE
:13,7	9F	:17,7	BF	:1B,7	DF	:1F,7	FF

*DC,FC= Device Address, Function Code

Appendix C

ALPHA I/O COMMANDS

C.1 GENERAL

Table C-1 lists the I/O commands applicable to the NAKED MINI/ALPHA LSI series computers. Note that this controller can only be used with an ALPHA LSI series computer.

Table C-1. Alpha I/O Command List

ALPHA 16 and LSI series	ALPHA 8	FUNCTION
INA :58	INA :58	Unconditional Input
INX :5A		
IBA :78		
IBX :7A		
INAM :5C	MIA :5C	
INXM :5E		
IBAM :7C		
IBXM :7E		
RDA :59	IAS :59	Conditional Input
RDX :5B		
RBA :79		
RBX :7B		
RDAM :5D	MIS :5D	
RDXM :5F		
RBAM :7D		
RBXM :7F		
OTA :6C	OTA :6C	Unconditional Output
OTX :6E		
OTZ :68	OTZ :68	
WRA :6D	OAS :6D	Conditional Output
WRX :6F		
WRZ :69	OZS :69	
BIN :71		Block I/O
BOT :75		
AIN :50	AIN :5A	Auto I/O
AIB :54		
AOT :60	AOT :6E	
AOB :64		
SEA :44	SEA :44	Select and Present A
SEX :46		
SEL :40	SEL :40	
SEN :49	SEN :49	
SSN :48	SSN :48	

Appendix D

RECOMMENDED DEVICE AND INTERRUPT ADDRESSES

D.1 GENERAL

Table D-1 and D-2 list recommended Device and Interrupt Addresses to prevent possible conflict during future expansion to other I/O modules.

Table D-1. Recommended Device Addresses

DEVICE	DEVICE ADDRESSES	
	STANDARD	ACTUAL
Refer to Table D-3*	00	
	01	
Dual TTY/CRT (TTY1/CRT1)	02	
Dual TTY/CRT (TTY0/CRT0)	03	
Line Printer (LP)	04	
Card Reader (CR)	05	
Paper Tape Punch (PTP)	06 (17)	
Paper Tape Reader (PTR)	06	
Processor TTY* (TTY)	07	
Real Time Clock* (RTC)	08	
Magnetic Tape (Mag Tape)	09	
	0A	
	0B	
	0C	
Synchronous Modem Controller (SCM)	0D	
Asynchronous Modem Multiplexer (AMM)	0E	
Disk	0F	
Cassette	10	
	11	
16-Bit I/O (A/D System)	12	
	13	
Plotter	14	
	15	
32-Bit Relay In (RCIM)	16	
Punch Alternate	17	
16-Bit Input/Output (16-Bit I/O)	18	
64-Bit Input (64-Bit In)	19	
64-Bit Output (64-Bit Out)	1A	
Priority Interrupt Module (PIM)	1B	
32-Bit Relay Out (RCOM)	1C	
103 Data Set Controller (103 DSC)	1D	
	1E	
	1F	

* not alterable

( ) Indicates suggested alternate.

Table D-2. Scratchpad/Page 0, Recommended Interrupt Address Map

	00-1F	20-3F	40-5F	60-7F	80-9F	A0-BF	C0-DF	E0-FF
0	:00* Power Up	:20* 64-Bit Out	:40	:60 ACUM ACR 1	:80 PIM(0)	:A0	:C0 AMM RCV1 AMC RCV	:E0
2	TTY Word Note 4 TTY Xmit Word Note 5	Mag Tape Word TTY Recv. Word Note 5	LP Word	ACUM DSS1 TTY0 /CRT0 Word	PIM(1)	Plotter Word		
4				ACUM PND 1	PIM(2)		AMM XMIT1 AMC XMIT	
6	TTY EOB Note 4 TTY Xmit EOB Note 5	Mag Tape EOB TTY Recv. EOB Note 5	LP EOB	TTY0 /CRT0 EOB	PIM(3)	Plotter EOB		
8		PTR/PTP Word		ACUM ACR 2	PIM(4)		AMM RCV2	
A	M.H. Disk		CR Word	ACUM DSS 2 TTY1 /CRT1 Word	PIM(5)	RCIM Word		
C				ACUM PND 2	PIM(6)		AMM XMIT2	
E		PTR/PTP EOB	CR EOB	TTY1 /CRT1 EOB	PIM(7)	RCIM EOB		
0	:10* 64-Bit In.	:30 103 DSC Answer Auto Load	:50 Cassette Address	:70 ACUM ACR 3	:90 PIM(8) SMC Exception	:B0	:D0 AMM RCV3	:F0
2		103 DSC Input Word	Cassette Word	ACUM DSS 3 16-Bit I/O Word	PIM(9) SMC Input Word	AMM/AMC Exception		
4				ACUM PND3	PIM(10)	AMM/AMC Receive EOB	AMM XMIT3	
6		103 DSC In EOB	Cassette EOB	16-Bit I/O EOB	PIM(11) SMC Input EOB	AMM/AMC Transmit EOB		
8	RTC Clock	103 DSC Par Err /Flt		ACUM ACR 4	PIM(12) SMC Output Word		AMM RCV4	
A	RTC Sync.	. 103 DSC Output Word	RCOM Word	ACUM DSS4 16-Bit I/O Word	PIM(13)			
C	Power Down			ACUM PND 4	PIM(14) SMC Output EOB		AMM XMIT4	
E	CONS Int. & Trap.	103 DSC Out EOB	RCOM EOB	16-Bit I/O EOB	PIM(15)			

1. *Address cannot be changed.
2. EOB = End-of-Block
3. Split Address blocks and/or a/ indicate that this is the standard I/O vector for more than one device. Only one device may use a vector in any given system.
4. Half Duplex
5. Full Duplex

Appendix E

SPECIFICATIONS

E.1 GENERAL

The following specifications relate to the Moving Head Disk controller only. For specifications relating to the disk drive(s) used, refer to the manual(s) supplied with the disk drive(s).

E.2 DISK DRIVES SUPPORTED

The Moving Head Disk controller is capable of supporting a maximum of four of the following types of disk drives:

1. Diablo model 30 series
2. Diablo model 40 series
3. Other disk drives which are functionally electrically, and connector compatible to Diablo model 30 and 40 series drives.

E.3 LOGIC LEVELS

Internal logic levels

True = +2.6 to +5.0 Vdc
False = 0.0 to +0.45 Vdc

External logic levels

To/From Processor: True = 0.0 to +0.45 Vdc
False = +2.6 to +5.0 Vdc

To/From disk drive: Mostly negative true signals (same as To/From Processor above), but positive true in some cases. Refer to logic diagrams and disk drive manual(s).

E.4 AC POWER REQUIREMENT

None

E.5 DC POWER REQUIREMENT

5 Vdc @ 6.5 A
(both PC boards)

E.6 OPERATING TEMPERATURE

0 to +50 C

E.7 OPERATING HUMIDITY

5% to 90% relative, non-condensing

E.8 DIMENSIONS (each PC board)

Width 15 inches
Length 16.5 inches
Height 0.5 inches

Controller occupies 2 full PC board slots

Appendix F

INTERBOARD AND INTERFACE CONNECTORS

F.1 GENERAL

Four connectors are associated with the Moving Head Disk controller, two on each PC board. The 530 board has an interboard connector and a test connector. (The test connector is intended for factory use only.) The 531 board has an interboard connector and an interface connector. The pin assignments for each connector are listed in tables F-1 through F-3.

Table F-1. Test Connector P31 (530 Bd.) Pin Assignments

PIN	MNEMONIC	PIN	MNEMONIC	PIN	MNEMONIC	PIN	MNEMONIC
A01		A26		B01		B26	
A02	TPA02	A27		B02		B27	
A03	TPA03	A28		B03		B28	
A04	TPA04	A29		B04		B29	
A05	TPA05	A30		B05		B30	
A06	TPA06	A31		B06		B31	
A07	TPA07	A32	TPA32	B07		B32	
A08	TPA08	A33	TPA33	B08		B33	
A09	TPA09	A34	TPA34	B09		B34	
A10	TPA10	A35	TPA35	B10		B35	
A11	TPA11	A36		B11		B36	
A12	TPA12	A37		B12		B37	
A13	TPA13	A38	TPA38	B13		B38	
A14	TPA14	A39	TPA39	B14		B39	
A15	TPA15	A40	TPA40	B15		B40	
A16	TPA16	A41	TPA41	B16		B41	
A17	TPA17	A42	TPA42	B17		B42	
A18	TPA18	A43	TPA43	B18		B43	
A19	TPA19	A44	TPA44	B19		B44	
A20	SECCOM-	A45	TPA45	B20		B45	
A21		A46	TPA46	B21		B46	
A22	TPA22	A47	TPA47	B22		B47	
A23	DCS2-	A48	TPA48	B23		B48	
A24		A49	TPA49	B24		B49	
A25		A50	TPA50	B25		B50	

Table F-3. Interface Connector P11 (531 Bd.) Pin Assignments

PIN	MNEMONIC	PIN	MNEMONIC	PIN	MNEMONIC	PIN	MNEMONIC
A01	PS0	A26	SS03-	B01		B26	RESTE-
A02	PS1	A27	SS04-	B02	GND	B27	CAE, RESTE RET
A03	PS2	A28	JMP-	B03	GND	B28	CAE-
A04	PS3	A29		B04	WPTOUT-	B29	RDGD-
A05	PS4	A30	JMP2-	B05	SCPOL	B30	WRGT, RDGD RET
A06	E8-	A31	JMP3-	B06	SEKPL-	B31	WRGT-
A07	E16-	A32	JMP4-	B07	SEKPL RET	B32	WDAC4-
A08	E32-	A33	JMP5-	B08	ADACK-	B33	WDAC3, WDAC4 RET
A09	E64-	A34	BUS0-	B09	SECTX, ADACK RET	B34	WDAC3-
A10	E128-	A35	BUS0, BUS1 RET	B10	SECTX-	B35	WDAC2-
A11	E256-	A36	BUS1	B11	INDXB-	B36	WDAC1, WDAC2 RET
A12	E4-	A37	BUS2-	B12	UNSAFX, INDXB RET	B37	WDAC1-
A13	E2-	A38	BUS2, BUS3 RET	B13	UNSAFX-	B38	CNTLTG-
A14		A39	BUS3-	B14	SEKER-	B39	HEADTG, CNTLTG RET
A15	WRPTCT-	A40	BUS4-	B15	SEKER, DRDYX RET	B40	HEADTG-
A16	2SECCL	A41	BUS4, BUS5 RET	B16	DRDYX	B41	HSEL2-
A17	SECTX	A42	BUS5-	B17	RDACK3-	B42	HSEL1, HSEL2 RET
A18	10 STRAP	A43	BUS6-	B18	RDACK2, RDACK3 RET	B43	HSEL1-
A19	ERGT-	A44	BUS6, BUS7 RET	B19	RDACK2-	B44	SELECT 3-
A20	ERGT RET	A45	BUS7-	B20	RDACK1-	B45	SELECT 2, SELECT 3 RET
A21	20 STRAP	A46	SC0M0-	B21	RDACK0, RDACK1 RET	B46	SELECT 2-
A22	4 STRAP	A47	SCM0RT, 1RT, 1RT	B22	RDACK0-	B47	SELECT 1-
A23	SS00-	A48	SC0M1-	B23	DCLK-	B48	SELECT 0, SELECT 1 RET
A24	SS01-	A49	SC0M2-	B24	DDATA, DCLK RET	B49	SELECT 0-
A25	SS02-	A50	SCM3RT	B25	DDATA-	B50	SC0M3

Table F-2. Interboard Connectors P22 and P12 (530 & 531 Bd.) Pin Assignments

PIN	MNEMONIC	PIN	MNEMONIC	PIN	MNEMONIC	PIN	MNEMONIC
A01	CF07	A26		B01	DC500	B26	DCCL
A02	RDATA-	A27	DMARQA	B02	TR00A	B27	DMRQRT
A03	SECM1	A28	WDAT	B03	WD-	B28	WDATRT
A04	F1CLK-	A29	SECTB-	B04	F1CKRT	B29	STB
A05	HSEL1	A30	F2CLK-	B05	RD-	B30	F2CKRT
A06	HSEL0	A31	INDEX	B06	SEEK	B31	DC4
A07	SE00	A32	INZX-	B07	SEKCOM	B32	RI-
A08	SE01	A33	DEN2-	B08	HAERR	B33	DATA
A09	SE02	A34	ADACK	B09	CNT = 0-	B34	DS
A10	SE03	A35	JKCLK1	B10	RGA	B35	JKCKRT
A11	SE04-	A36	SRCLK2	B11	WGA	B36	SRCKRT
A12		A37	ECA	B12	CCW00	B37	ICSCMP
A13		A38		B13	LS00	B38	DACCE
A14		A39	RCLK-	B14	DNRTIM	B39	RCLKRT
A15		A40	WF-	B15	SEEKER	B40	TR04
A16		A41	RV-	B16	UNSAFE-	B41	TR03
A17		A42		B17	0EVEN	B42	TR02
A18		A43	RESTE	B18	SCA	B43	TR01
A19		A44	OTBS0	B19	SHA	B44	OTBS7
A20		A45	OTBS1	B20	DEXEC	B45	JMP-
A21		A46	OTBS2	B21	SF	B46	TRSA
A22		A47	OTBS3	B22	2IDX-	B47	JMP2-
A23		A48	OTBS4	B23	IDCCE	B48	JMP3-
A24		A49	OTBS5	B24	DCCC	B49	JMP4-
A25		A50	OTBS6	B25	DRCEN-	B50	JMP5-

Appendix G

STANDARD I/O INTERFACE PIN ASSIGNMENTS

G.1 GENERAL

Table G-1 lists the standard I/O interface pin assignments found on the NAKED MINI/ALPHA LSI motherboard.

Table G-1. Standard I/O Interface Pin Assignments

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN.	FUNCTI
101	GND	144	+5V	201	GND	244	+5V
102	GND	145	DB04-	202	GND	245	DB04-
103	+12V	146	DB05-	203	+12V	246	DB05-
104	+12V	147	DB06-	204	+12V	247	DB06-
105	+12V	148	DB07-	205	+12V	248	DB07-
106	+12V	149	DB08-	206	+12V	249	DB08-
107	-12V	150	DB09-	207	-12V	250	DB09-
108	-12V	151	DB10-	208	-12V	251	DB10-
109		152	DB11-	209	DPIN-	252	DB11-
110		153	DB12-	210	DPOT-	253	DB12-
111		154	DB13-	211		254	DB13-
112		155	DB14-	212		255	DB14-
113	+5V	156	DB15-	213	+5V	256	DB15-
114	+5V	157	EXEC-	214	+5V	257	EXEC-
115	MST-	158	IN-	215	MST-	258	IN-
116		159	GND	216		259	GND
117	MACK-	160	GND	217	MACK-	260	GND
118	RD-	161	IOCL-	218	RD-	261	IOCL-
119		162	OUT-	219	TYP1-	262	OUT-
120	SLB-	163	CLK-	220	SLB-	263	CLK-
121	PFD-	164	SER-	221	PFD-	264	SER-
122	MDIS-	165	IUR-	222	MDIS-	265	IUR-
123	AB08-	166	IL1-	223	AB08 -	266	IL1-
124	AB09-	167	IAR-	224	AB09 -	267	IAR-
125	AB10-	168	IL2-	225	AB10 -	268	IL2-
126	AB11-	169	RST-	226	AB11 -	269	RST-
127	GND	170	IUA-	227	GND	270	IUA-
128	GND	171	PLSE-	228	GND	271	PLSE-
129	AB12-	172	ECHO-	229	AB12-	272	ECHO-
130	AB13-	173	+5V	230	AB13-	273	+5V
131	AB14-	174	+5V	231	AB14-	274	+5V
132	AB15-	175	AB03-	232	AB15-	275	AB03-
133		176	AB04-	233		276	AB04-
134		177	AB05-	234		277	AB05-
135	STOP-	178	AB06-	235	STOP-	278	AB06-
136	SACK-	179	AB07-	236	SACK-	279	AB07-
137		180	AB00-	237	MBIN-	280	AB00-
138		181	AB01-	238	MBOT-	281	AB01-
139	DB00-	182	AB02-	239	DB00-	282	AB02-
140	DB01-	183	PRIN-	240	DB01-	283	PRIN-
141	DB02-	184	PROT-	241	DB02-	284	PROT-
142	DB03-	185	GND	242	DB03-	285	GND
143	+5	186	GND	243	+5	286	GND

Appendix H

DIABLO MODELS 31 AND 33 INTEGRATION SPECIFICATIONS

H.1 GENERAL

In order to properly integrate the Diablo Model 31 or 33 disk drive into the Computer Automation Moving Head Disk system, it is necessary to do the following:

1. Order necessary device options from Diablo, as described in paragraph H.1.1.
2. Configure Diablo Disk Drive PC boards, as described in paragraph H.1.2.

Note that the Moving Head Disk controller is capable of supporting up to four units, where a model 31 counts as one unit, and the model 33 as two units. The models may be intermixed as long as the total number does not exceed four. The two models are configured as follows:

Diablo Model 31 - Single platter, removable
Diablo Model 33 - Dual platter; one fixed, one removable.

H.1.1 Necessary Options

Table H-1 lists the necessary device options for disk drive models 31 and 33 which should be obtained from Diablo System Inc. The options to be ordered with each model are noted by an X in the associated model number column. Quantity, if more than one, is indicated in parenthesis.

Table H-1. Device Options

OPTION NO.	DESCRIPTION	MODEL 31	MODEL 33
004	Standard High Density	X	X
005	Write Protect	X	X
018	Standard Flush Mounting	X	X
029	Dual Power Supply	X	X

Table H-1. Device Options (Cont'd)

OPTION NO.	DESCRIPTION	MODEL 31	MODEL 33
032	Power Cable	X	X (2)
036	Pin Terminator	X	X
042	High Density 24-Sector Disk Pack	X	X (2)
044	Power Supply Rack Mounting	X	X
045	Black Bezel, No Logo	X	X
047	Attention Line - Negative	X	X
053	Receptacle/Pin Interconnect Cable	(Note 3)	X (Note 3)

Notes:

1. Only one Pin Terminator (option 036) is required per disk controller (up to four disk drives).
2. One Dual Power Supply (option 029) will support two model 31 disk drives or one model 33 disk drive.
3. One Receptacle Pin Interconnect cable (option 053) is required for each additional model 31 or model 33 attached to the disk controller.

H.1.2 PC Board Configurations

Table H-2 lists the PC boards within the Diablo Disk Drive(s) and the components which are to be installed or removed to ensure proper operation with the Moving Head Disk Controller.

Table H-2. Diablo PC Board Configuration

SCHEMATIC	PC BOARD AND COMPONENT LOCATION	COMPONENT	INSTALL OR REMOVE
11111	J2-K12	680 Ω Resistor	Remove
	-A15	10 Ω Resistor	Remove
	-B16	10 Ω Resistor	Install
11111	-K13	4.7k Resistor	Install
11026	J3-A10	Jumper Wire	Install
	-A15	"	Install
	-A13	"	Remove
	-H28	150Ω , ¼W Resistor	Remove
	-H30		
	-H20		
	-H15		
	-H23		
	-H18		
	-H10		
	-H5		
	-H13		
11026	-H8	150Ω , ¼W Resistor	Remove
11071	J9-A24	IC 936	Install if Write Protect used
	-B24	IC 946	
	-F14	1.5k Resistor	
	-E14	Diode 1N4454	
	-E13	15k Resistor	
	-E11	Transistor 2N3641	
	-E8	22 Ω Resistor	
	-E7	270 Ω , ¼W Resistor	
	-E16	470 Ω , ¼W Resistor	
	-A16	270 Ω Resistor	
	-B15	0.1 µ F Capacitor	
11071	-A14	150 Ω , ¼W Resistor	Install if Write Protect used
11071	J9-E7	22 Ω , ¼W Resistor	Install if Write Protect not used

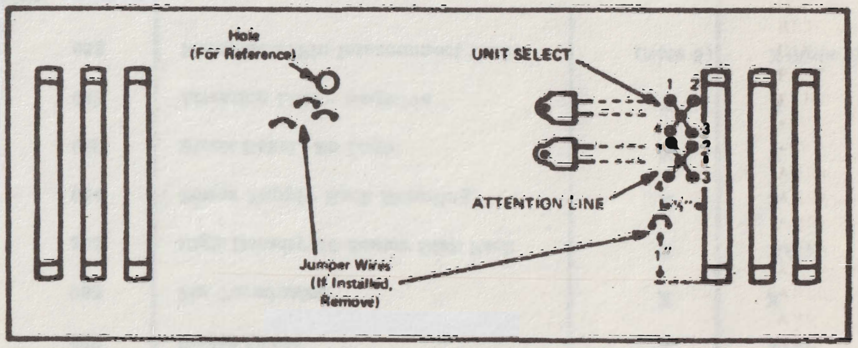
---

Table H-2. Diablo Model 30 Series PC Board Configurations (Cont'd)

SCHEMATIC	PC BOARD AND COMPONENT LOCATION	COMPONENT	INSTALL OR REMOVE
11082	J10-F9	10Ω Resistor	Install
	-F41	150 Ω , ¼W Resistor	Remove
	-D44		
	-H41		
	-D39		
	-E42	150 Ω , ¼W Resistor	Remove
	-K28	10Ω Resistor	Install
11082	-F39	10Ω Resistor	Remove
	Motherboard	Jumper wires	Remove (see figure H-1)
	Motherboard	Select and Attention jumper plugs	Install (see figure H-1)

Notes:

1. Refer to Diablo Model 31 Maintenance manual for general descriptions of component references.
2. All resistor ¼W unless otherwise stated.



Notes:

1. Install Unit Select & Attention Line jumper plugs between center jack and jack associated with unit no. Both plugs must relate to the same unit no.
2. For software purposes, unit 1 = Disk Drive 0, unit 2 = 1, unit 3 = 2, and unit 4 = 3.

Figure H-1. Diablo Models 31 and 33 Motherboard Configuration

Appendix I

DIABLO DISK DRIVE CONSIDERATIONS

The Diablo Model 43 or 44 disk drives used with the Computer Automation Moving Head Disk System must contain Diablo PC boards configured as shown in Table I-1 (Model 43) or Table I-2 (Model 44). Any discrepancy between the tables and the disk drive should be referred to Diablo Systems Incorporated, Hayward, California. The I/O and main card cages are shown in Figures I-1 and I-2, respectively.

The read/write heads alignment procedure specified in the Diablo Maintenance Manual (D40-173, 1971 paragraph 3.20 or 81601 paragraph 6.6.4.3) must be performed to insure interchangability of disk packs written on different drives. This procedure must be followed whenever the drives have been transported.

To insure complete up to date service information is in their possession it is recommended that the end user solicit from Diablo Systems, Inc. all Diablo Field Service Aid bulletins and request that their name be added to the Field Service and mailing list maintained by Diablo.

Reference should be made to Diablo Field Service Aid #10 if a disk drive of a lower serial number than #2604 is to be used. This is in regard to the SI board which should be retrofitted to these units.

If it is necessary to replace the OR boards (Diablo part number 11414-xx) care should be taken to insure that the jumpers at locations H50 thru H57 and J50 thru J57 on the new boards match the jumpers on the old boards.

Table I-1 Model 43

DIABLO BOARD LOCATION	SCHEMATIC NUMBER	MNEMONIC	COMPONENT LOCATION NUMBER	COMPONENT TYPE	INSTALLED OR REMOVED
IO1	(11431-01)		E22	.47μh Inductor	Removed
IO1	(11643-01)	RDR1	A5	10 Ω, 1/4W Resistor	Installed
			A10, D10	10 Ω, 1/4W Resistor	Removed
			E22	Jumper	Removed
IO3	(11459)	SC		Entire Board	Installed
IO5	(11429-01)	DCS	A17, D3	62 pf Capacitors	Installed in place of 100 pf
			D6, D9	8.25K, 1/8W 1% Resistor	Installed in place of 10.5K
			E6	120 Ω, 1/2W Resistor	Removed
			E7	300 Ω, 1/2W Resistor	Removed
IO5	(11637-01)	DCS	D3, D13	62 pf, ±5% cap	Installed in place of 100 pf
			D6, D9	8.25K, 1/8W 1% Resistor	Installed in of 10.5KΩ
			F10	10 Ω, 1/4W Resistor	Removed
IO2	(11433)		Must have 11433 assembly number stamped on board. NO OPTIONS FOR THIS VERSION OF IO2 CARD.		
IO2	(11645-00)	RDR2	A21, B21	Jumper or Resistor	Removed
			D21	Jumper	Installed
			Must have 11645-00 assembly number stamped on the board.		

Table I-1 Model 43 (Cont'd)

DIABLO BOARD LOCATION	SCHEMATIC NUMBER	MNEMONIC	COMPONENT LOCATION NUMBER	COMPONENT TYPE	INSTALLED OR REMOVED
IO4			Spare, no card installed.		
IO6			Spare, no card installed.		
M01	(11416)	SD	H6	3 Megohm 1/4W Resistor	Installed in place of 1M, 1/4W, Resistor
M01	(11613-00)	SD	E48	10Ω, 1/4W Resistor or Jumper	Installed
			E56	10Ω, 1/4W Resistor or Jumper	Removed
			H6	3 Megohm 1/4W Resistor	Installed in in place of 1M, 1/4W, Resistor
M02	(11414-01)	OR	H22	10Ω, 1/4W Resistor	Installed
M03			Spare, no card installed.		
M04			Spare, no card installed.		
M05	(11409-01 or 11471-01)	SL	A34	102K Ω, 1% Resistor	Installed in place of 158K
M06	(11411-01, J or earlier revisions	SR	F30, F32, F35	Jumper or 10Ω, 1/4W Resistor	Removed
			F31, F33, F34	Jumper or 10Ω, 1/4W Resistor	Installed
M06	(11411-01, K or later revisions	SR	F29, F31, F35	Jumper or 10Ω, 1/4W Resistor	Removed
			F30, F32, F34	Jumper or 10Ω, 1/4W Resistor	Installed

Table I-1 Model 43 (Cont'd)

DIABLO BOARD LOCATION	SCHEMATIC NUMBER	MNEMONIC	COMPONENT LOCATION NUMBER	COMPONENT TYPE	INSTALLED OR REMOVED
M07	(11402)	SO	E37	.47 µf cap	Removed
			E38	1.21 M, 1/4W 1% Resistor	Removed
			J9	On some machines was 75K Ω, 1%. Should be 86.5K or 87.7K Ω, 1% Resistor	
M07	(11633-00)	SO	E37	.47 µf cap	Removed
			E38	1.21 M, 1/4W 1% Resistor	Removed
M08	(11407-00)	AL2	J55, J57	Jumper	Installed
			J54, J56	Jumper	Removed
M09	(11404-00)	AL1	D3	Jumper	Removed
			J39	270 pf cap	Installed in place of .003 µf cap
			J44	300 pf cap	Installed in place of .001 µf cap
			J41	5.1K, 1/4W, 5% Resistor	Installed in place of 33K
			J45	10K, 1/4W, 5% Resistor	Installed in place of 15K

Table I-1 Model 43 (Cont'd)

DIABLO BOARD LOCATION	SCHEMATIC NUMBER	MNEMONIC	COMPONENT LOCATION NUMBER	COMPONENT TYPE	INSTALLED OR REMOVED
Heatsink Assembly	(11418 or 11631-00)	HS HS	H78	IN4454 Diode	In parallel with diode type A14A
			E27	Zener Diode Assembly (two 6.2V zeners with cathodes tied together) installed in placeof a resistor.	
			E33	No component installed.	
Data Channel Box	(11486-00)	R/W	J94, J104	.022 µf	Installed in place of .033 µf cap
			E105	510 pf cap	Installed in place of .001 µf cap
			H95, H105	39 pf cap	Installed in place of 62 pf cap
			H94, H104, J99	120 pf cap	Installed in place of 180 pf cap
			E94	150 pf cap	Installed in place of 240 pf cap
			H96, H106	4.7 µH choke	Installed in place of 6.8 µH choke

Table I-1 Model 43 (Cont'd)

DIABLO BOARD LOCATION	SCHEMATIC NUMBER	MNEMONIC	COMPONENT LOCATION NUMBER	COMPONENT TYPE	INSTALLED OR REMOVED
Data Channel Box (cont.)	(11486-00)	R/W	H93, H97, H100 H103	22 µH choke	Installed in place of 33 µH choke
			B75	165 Ω, 1/2W 1% Resistor	Installed in place of 86.6 Ω, 1%, 1/2W
			B92, B93	470 Ω, 1/4W 5% Resistor	Installed in place of 430 Ω, 1/4W
			J102	620 Ω, 1/4W 5% Resistor	Installed in place of 330 Ω, 1/4W
			E108	1.3K Ω, 1/4W	Installed in place of 1.5K Ω, 1/4W
			D111	2.0K Ω. 1/4W 5% Resistor	Installed
			A72	5.6K Ω, 1/4W 5% Resistor	Installed in place of 10K Ω, 1/4W
			E107	Jumper	Installed
			E10, E11	10Ω, 1/4W Resistor	Removed

Table I-2 Model 44

DIABLO BOARD LOCATION	SCHEMATIC NUMBER	MNEMONIC	COMPONENT LOCATION NUMBER	COMPONENT TYPE	INSTALLED OR REMOVED
IO1	(11643-01)	RDR1	A5	10Ω, 1/4W Resistor	Installed
			A10, D10	10Ω, 1/4W Resistor	Removed
			E22	Jumper	Removed
IO3	(11459)	SC		Entire Board	Installed
IO5	(11429-01)	DCS	A17, D3	62 pf Capacitors	Installed in place of 100 pf
			D6, D9	8.25K, 1/8W 1% Resistor	Installed in place of 10.5K
			E6	120Ω, 1/2W Resistor	Removed
			E7	300Ω, 1/2W Resistor	Removed
IO5	(11637-01)	DCS	D3, D13	62 pf, 5% cap	Installed in place of 100 pf
			D6, D9	8.25K, 1/8W 1% Resistor	Installed in place of 10.5K
			F10	10Ω, 1/4W Resistor	Removed
IO2	(11647-00)	RDR2	Must have 11647-00 assembly number stamped on the board.		
			B11, B21	Jumper or Resistor	Removed
			B20	Jumper	Installed
IO4,6			Spare - No card installed.		

Table I-2 Model 44 (Cont'd)

DIABLO BOARD LOCATION	SCHEMATIC NUMBER	MNEMONIC	COMPONENT LOCATION NUMBER	COMPONENT TYPE	INSTALLED OR REMOVED
M01	(11416)	SD	H6	3Megohm 1/4W resistor	Installed in place of 1M, 1/4W, resistor
M01	(11613-00)	SD	E48	10Ω, 1/4W Resistor or Jumper	Installed
			E56	10Ω, 1/4W Resistor or Jumper	Removed
			H6	3Megohm 1/4W resistor	Installed in place of 1M, 1/4W, resistor
M02	(11414-01)	OR	H22	10Ω, 1/4W Resistor	Installed
M03			Spare - No card installed.		
M04	(11537)	TC	Entire Board		Installed
M05	(11409-01 or 11471-01)	SL	A34	102KΩ, 1% Resistor	Installed in place of 158KΩ
M06	(11411-01, J or earlier revisions)	SR	F30, F32, F35	Jumper or 10Ω, 1/4W Resistor	Removed
			F31, F33, F34	Jumper or 10Ω, 1/4W Resistor	Installed
M06	(11411-01, K or later revisions)	SR	F29, F31, F35	Jumper or 10Ω, 1/4W Resistor	Removed
			F30, F32, F34	Jumper or 10Ω, 1/4W Resistor	Installed

Table I-2 Model 44 (Cont'd)

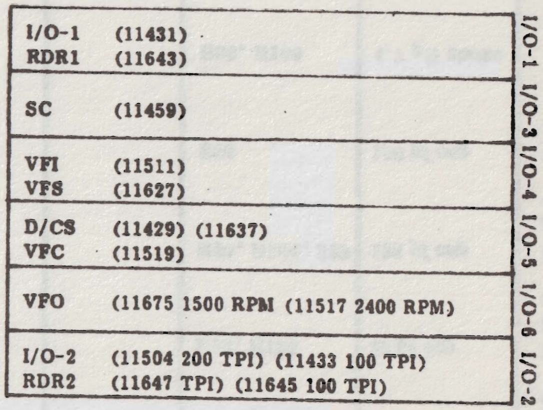
DIABLO BOARD LOCATION	SCHEMATIC NUMBER	MNEMONIC	COMPONENT LOCATION NUMBER	COMPONENT TYPE	INSTALLED OR REMOVED
M07	(11402-20)	SO	E37	.47 µf cap	Installed
			E38	1.21M, 1/4W 1% Resistor	Installed
			J9	On some machines: was 75KΩ, 1%/ Should be 86.6K or 87.7KΩ, 1% Resistor	
M07	(11633-20)	SO	E37	.47 µf cap	Installed
			E38	1.21M, 1/4W 1% Resistor	Installed
M08	(11407-20)	AL2	J55, J57	Jumper	Removed
			J54, J56	Jumper	Installed
M09	(11404-20)	AL1	D3	Jumper	Installed
			J39	270 pf cap	Installed in place of .0033 f cap
			J44	300 pf cap	Installed in place of .001 f cap
			J41	5.1K, 1/4W, 5% Resistor	Installed in place of 33K
			J45	10K, 1/4W, 5% Resistor	Installed in place of 15K

Table I-2 Model 44 (Cont'd)

DIABLO BOARD LOCATION	SCHEMATIC NUMBER	MNEMONIC	COMPONENT LOCATION NUMBER	COMPONENT TYPE	INSTALLED OR REMOVED
Heatsink Assembly	(11418, or 11631-00)	HS	H78	IN4454 Diode	In parallel with diode type A14A
			E27	Zener Diode Assembly (two 6.2V zeners with cathodes tied together) in place of a resistor.	
			E33	No component installed.	
Data Channel Box	(11486-20)	R/W	J94, J104	.022 µf	Installed in place of .003 µf cap
			E106	.001 µf cap	Installed in place of 510 pf cap
			H95, H105	39 pf cap	Installed in place of 62 pf cap
			H94, H104, J99	120 pf cap	Installed in place of 180 pf cap
			E94	150 pf cap	Installed in place of 240 pf cap
			H96, H106	4.7 µH choke	Installed in place of 6.8 µH choke
			H93, H97, H100, H103	22 µH choke	Installed in place of 33 µH choke

Table I-2 Model 44 (Cont'd)

DIABLO BOARD LOCATION	SCHEMATIC NUMBER	MNEMONIC	COMPONENT LOCATION NUMBER	COMPONENT TYPE	INSTALLED OR REMOVED
Data Channel Box (cont.)	(11486-20)	R/W	B75	86.6 Ω, 1/2W 1% Resistor	Installed in place of 165Ω, 1%, 1/2W
			B92, B93	330 Ω, 1/4W 5% Resistor	Installed in place of 470Ω, 1/4W
			J102	330Ω, 1/4W 5% Resistor	Installed in place of 620 Ω, 1/4W
			E108	1.5 Ω, 1/4W	Installed in place of 1.3Ω, 1/4W
			D111	2.0K Ω, 1/4W 5% Resistor	Installed
			A72	10K Ω, 1/4W 5% Resistor	Installed in place of 5.6KΩ, 1/4W
			E107	Jumper	Installed
			E10, E11	10 Ω, 1/4W Resistor	Removed

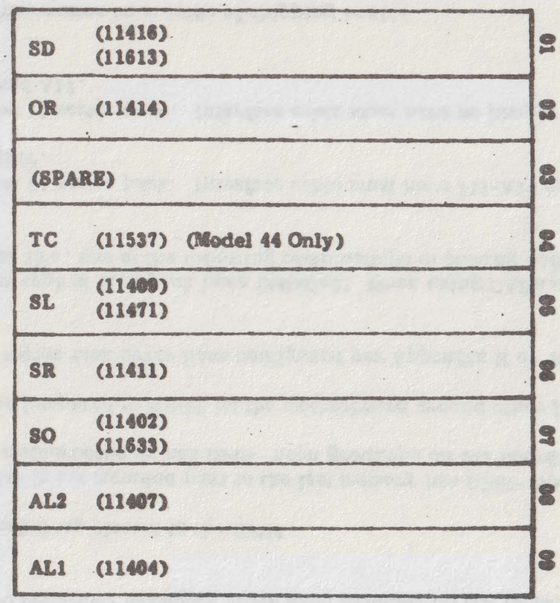

I/O-1 (11431)
RDR1 (11643)
SC (11459)
VFI (11511)
VFS (11627)
D/CS (11429) (11637)
VFC (11519)
VFO (11675 1500 RPM (11517 2400 RPM)
I/O-2 (11504 200 TPI) (11433 100 TPI)
RDR2 (11647 TPI) (11645 100 TPI)
I/O-1
I/O-3
I/O-4
I/O-5
I/O-6
I/O-2

I/O CARD CAGE
(As Viewed From The Front)

Figure I.1

NOTES:

1. This applies to 11521 Motherboard only.
2. For 11400 Motherboard D/CS is mounted left one slot.
3. The following cards are not used by CAI: VFI, VFS, VFC, VFO.


SD (11416) (11613)
OR (11414)
(SPARE)
TC (11537) (Model 44 Only)
SL (11409) (11471)
SR (11411)
SO (11402) (11633)
AL2 (11407)
AL1 (11404)
01
02
03
04
05
06
07
08
09

MAIN CARD CAGE
(As Viewed From the Front)

Figure I.2

Appendix J

INSTALLATION CHECK LIST

1. Does Processor run QCD (IDP, memory, and I/O)?

2. Is disk controller mounted next to last memory and do all memories have their shields installed.

3. Does 530 board have crystal installed and is crystal 3.124 MHz (for Model 30) or 5.000 MHz (for Model 40)?

4. Does 531 board have 10MHz crystal installed?

5. Has interface cable connector been installed on 531 board right hand side?

6. Has interboard connector assembly 53546 been installed on left hand side of 530/531 boards?

7. Is the side labeled top closest to the CPU?

8. If the controller is not mounted next to the last memory has DPIN- been jumpered on processor motherboard or has DPIN- been grounded on 531 board?

9. Has MBIN been jumpered to MBOT on the motherboard around other I/O cards?

10. Has Model 30 series disk drive been configured per Appendix H or 40 series per Appendix I?

11. Has the proper type of disk pack been installed? When using CAI's standard software for Model 30's, one of the following combinations of cabling and packs must exist:

    A. Mechanical 24 sector pack: Interface cable must have J11-A16 and A17 tied together.

    B. Mechanical 12 sector pack: Interface cable must have no jumper between J11-A16 and A17.

    Do not trust information on outside of shipping box!!!

    For CAI's standard Model 40, only combination A is allowed.

12. The interface cable for a Model 40 is a 15264-02.
    For a Model 30 it is a 15264-01
    The -02 has a 50 pin connector; the -01, 42 pin.

13. Has the head restraint bar been removed from inside the drive?

14. For the Model 40, the "READY" indicator will not come on if any of the following is not right:

    A. Top (removable) pack and its dust cover installed.

    B. Cartridge holding clamps not closed.

    C. Equipment drawer not completely closed (not all the way in on slides).

    D. Takes 60-80 seconds to come ready after pushing LOAD/RUN switch.

    E. Power cable not connected.

    F. Head restraint removed.

15. For the Model 30 the "READY" indicator will not come on if any of the following is not right:

    A. Pack installed.

    B. Door closed.

    C. Head restraint removed.

    D. Power cable installed and AC cord plugged in.

    E. Takes 60 to 80 seconds to come ready after pushing the LOAD/RUN switch.

MOVING HEAD DISK DIAGNOSTIC

INTRODUCTION

The Moving Head Disk Diagnostic Program verifies the proper functioning of the Moving Head Disk Controller and its associated disk drives. The program may be run on the Alpha 16, LSI-1, or LSI-2 system without modification.

USAGE

The program resides on paper tape in absolute binary format and is loaded into memory using the Binary Loader (BLD) or Autoload, beginning at location 0. Once loaded, the P register should be set to : 200 or : 210 to begin execution.

TEST DESCRIPTIONS

Test A

This test checks the proper operation of the Write Format, Verify, and Read Identifier functions. Note that this test, if successful, also sets up the proper disk format for the other tests. Testing is done by issuing a Write Format function to each cylinder of the disk followed by a Verify CRC and a Read Identifier function. I/O status is checked for each operation and correct cylinder number data is compared for each Read Identifier function.

Test B (Not applicable to Alpha 16)

This test verifies the operation of the Read ID function for more than one header; specifically, that the function will continue to read past a head boundary, but will terminate upon an end-of-cylinder condition, given sufficient word length. The ID of each sector is three words in length:

Word 1,	Cylinder Number
Word 2,	Sector Number/Head Number
Word 3,	CRC Check Word

This is done by issuing a Read ID function to the first requested cylinder, head 0 for a word length of (number of sectors per track + 1) times 3, thus guaranteeing a read length which will cross a head boundary.

Then a second Read ID function is issued to the first requested cylinder, last head, for the same word length as the previous operation, guaranteeing that the end-of-cylinder condition occurs before the word count is exhausted. Correct input of each 3-word ID is also verified for each operation.

At the end of each test, the overflow indicator blinks, indicating the test program is still being executed.

Test C

This test checks for proper status after a Write, Verify, and Read operation to the disk. This is done by issuing each of the above functions to the first requested cylinder, first requested head, sector 0, using a data length of one word, after which a status check is performed to see that each I/O operation terminates properly. Correct data transfer is also checked.

At the end of each test, the overflow indicator blinks, indicating the test program is still being executed.

Test D

This test checks to see that the LSI-1 controller, for a Read function, enters the hog mode when the data transfer begins (subsequent to seeking the correct cylinder), and that a Read ID function enters the hog mode immediately (before seeking). It also tests to see that the LSI-2 controller does not enter the hog mode for either a Read or a Read ID.

If the controller is being tested in an LSI-1 processor, a Restore function is issued to return the heads to cylinder 0, followed by a timed Seek function to cylinder 200. The time should be less than 12.5% of the Seek time. Then another Restore function is issued, followed by a timed two-word Read function to cylinder 200. This time should be at least 87.5% of the Seek function.

If the controller is being tested in an LSI-2 or Alpha 16 processor, a Restore function is issued, followed by a timed Seek function to cylinder 200. This is followed by another Restore function and a timed Read ID function to cylinder 200. The times for the Seek and Read ID functions are then checked to see that they are within 87.5% - 112.5% of each other. This is followed by another Restore function, and a timed two-word Read function to cylinder 200 which should be at least 87.5% of the Seek time.

At the end of each test, the overflow indicator blinks, indicating the test program is st being executed.

NOTE

> Timing in test D is measured by incrementing a counter from zero, where each increment represents the time required to perform the following instructions:

```
CKSTAT     SSN                          (Sense I/O operation complete)
           LLL          16
           LLL          16              (Delay)
           IMS          *TIMPTR         (Increment counter)
           JMP          CKSTAT          (Repeat the sense test)
TIMPTR     DATA TIMER                   (Pointer to time count)
```

Test E

This test checks the operation of the disk using a data word supplied by the user. This is done by issuing a Write operation to each sector of each requested cylinder and head, using the user's pattern as data for each word of a sector. Checks are made for proper I/O termination. This procedure is then repeated using a Verify, then a Read, then a Hog Mode Read function code. For the Read and Hog Mode Read functions, correct data transfer is also verified.

Upon completion of each cylinder, the overflow indicator blinks indicating the test program is still being executed.

Test F

This test performs Write, Verify, and Read functions to each sector of each requested cylinder and head, using random adresses and random data. The cylinder, head, and sector sequencing is determined by accessing a pseudo-random number generator as follows:

(a) write to random cylinders, and within a given cylinder,
(b) write to random heads and within a given head,
(c) write to random sectors until each sector of the requested cylinders and heads has been written once and only once.

The same sequence of random addresses is then used to perform Verify and Read functions.

The data used is also generated from the pseudo-random number generator, and is statistically independent within a distance of one bit in either direction from the current bit in the serial bit stream. Correct data transfer is verified during the Read operations, and a data miscompare error report will include the random number used to generate the data.

Upon completion of each sector, the overflow indicator blinks indicating the test program is still being executed.

NOTE

This test may take up to two hours to complete, depending on the number of cylinders and heads present.

Test G

This test checks to see that the disk can accommodate I/O operations of more than one sector in length. This is done by issuing a Write operation to the last sector of each cylinder and head as follows. The data written is an incrementing pattern beginning with 0, and the data length of each operation is twice the given sector length. Each I/O operation is then repeated each time incrementing the head number until all requested heads except the last have been tested on a cylinder. Then the cylinder number is incremented and the entire process is repeated until all requested cylinders have been tested. The above is then repeated in the Verify mode and again in the Read mode, where correct data transfer is also verified.

Upon completion of each cylinder, the overflow indicator blinks indicating the test program is still being executed.

Test H

This test checks to see that a partial sector is written and read correctly. It also verifies the correctness of the CRC word. This is done by writing a 127-word record to sector 0 of the first requested cylinder and head, using the incremental data pattern 0 - : 7E. The actual functioning of the hardware is as follows (assume a 256 word per sector size): The first 127 words have the data pattern 0 - : 7E written to them. The last data word passed from memory (: 7E) continues to be written throughout the rest of the sector.

After the write operation is completed, the CRC word is input to memory. For the particular pattern used in this test, the CRC word should be : 0001. Then a read function is issued to input the entire sector into memory. The data is then checked to see that the correct pattern exists.

At the end of each test, the overflow indicator blinks indicating the test program is still being executed.

Test I, Section 1 (Section 1 not run if memory speed unspecified)

This section checks to see that the Seek only function performs correctly. This is done by selecting the disk to Restore to cylinder 0. Then a Seek function is issued to cylinder 0. There should be no movement of the heads, and therefore the operation should terminate within 100 microseconds. A Seek function is then issued to cylinder 200. The timing is checked to make sure the operation takes at least 30 milliseconds.

Test I, Section 2

This section consists of Read ID functions to different cylinders to verify that the correct cylinder has been found. The cylinder number used alternates between two counters. Counter A starts at zero, counter B starts at the maximum cylinder number. Counter A increments to the maximum cylinder number and Counter B decrements to cylinder zero. The ID is compared to the expected cylinder number for each I/O operation.

For example, the seek pattern for a 204-cylinder disk would be (in decimal):

Cylinder No.	Seek No.	Counter
0	1	A
203	2	B
1	3	A
202	4	B
2	5	A
201	6	B
3	7	A
200	8	B
.	.	.
.	.	.
200	401	A
3	402	B
201	403	A
2	404	B
202	405	A
1	406	B
203	407	A
0	408	B

Upon each incrementation of Counter A, the overflow indicator blinks indicating the test program is still being executed.

Test J

This test attempts to simulate the following error conditions in order to test the correct setting of the corresponding bits in the error status word:

1. Illegal sector address
2. Illegal head address
3. Illegal cylinder address

The illegal sector status is tested by issuing a 2-word Write function to the first requested cylinder and head, last sector plus one. The expected status is No ID Compare.

The illegal head status is tested by issuing a 2-word Write function to the first requested cylinder, sector 0, last head plus one. The expected status is Illegal Head Address and No ID Compare.

The illegal cylinder status is tested by issuing a 2-word Write function to head 0, sector 0, and last cylinder plus one. The expected status is Seek Error.

These three I/O operations are then repeated using a Read function code.

At the end of each test, the overflow indicator blinks indicating the test program is still being executed.

Test K (Not run if memory speed unspecified)

This test checks to see that resynchronization occurs on initial output when changing units. This is done by issuing a Read operation to the last sector of the requested cylinder and head of the current unit. Upon completion the Read head should be positioned just past the beginning of sector 0. Then a No-op command is issued for a different unit, after which a second Read function is issued to sector 1 of the current unit, on the same cylinder and head as the previous Read operation. Normally, a full rotation of the disk would not be necessary to position the heads for sector 1; however, the intervening selection of a different unit should cause resynchronization to occur, and thus the second Read operation should take at least one full revolution time to complete. Errors are output if completion takes less than 2 sector times (1 sector time for LSI-1), indicating that resynchronization did not occur, of if completion time is not within the range of from 1 revolution plus 1 sector times (1 rev + .5 sector times for LSI-1) through 1 revolution + 2.5 sector times, indicating that resynchronization did occur but the timing was incorrect.

At the end of each test, the overflow indicator blinks indicating the test program is still being executed.

Test L (not run if memory speed unspecified)

This test checks to see that resynchronization does not occur when switching to a different head on the same platter. This is done by issuing a read function to the last sector minus two of the current unit, for a length of one sector. The purpose of this I/O operation is to position the heads for the next Read operation, which is then issued to the last sector, for a length of two sectors. This causes head switching during the I/O operation. The time for the second operation is then checked to see that it is less than three sector times (1.5 sector times for LSI-1). If it is greater, it indicates that unexpected resynchronization occurred when head-switching on the same platter.

At the end of each test, the overflow indicator blinks, indicating the test program is still being executed.

Test M (Not run if memory speed unspecified, also requires at least 4 heads per unit)

This test verifies that resynchronization occurs when changing platters, if using a 40 series (4-headed) disk, and that resynchronization will not occur when changing platters, if the disk is not of the 40 series type.

This is done by issuing a Read operation to the last sector of an even numbered head, for a length of one sector. Then a second Read operation is issued to sector 1 of the next even numbered head (on a different platter). The time for the second operation is checked to see that it is greater than two sector times (1 sector time for the LSI-1) if the disk is a 40 series, and less than that time if it is not.

At the end of each test, the overflow indicator blinks indicating the test program is still being executed.

Test N (Not run if memory speed unspecified, also requires at least 4 heads per unit)

This test verifies that resynchronization will occur on a 40 series (4- headed) disk when crossing a platter boundary during an I/O operation, and that it will not occur if the disk is not of the 40 series type.

This is done by issuing a Read function to the last sector minus two of an odd numbered head, for a length of one sector. This is to position the heads for the next Read operation, which is issued to the last sector of the same head, for a length of two sectors (causing platter switching to the next head during the operation).

The time for the second operation is then checked to see that it is greater than 3 sector times (1 sector time for LSI-1) if a 40 series disk is being tested, or that it is less than that time if the disk is not of the 40 series type.

At the end of each test, the overflow indicator blinks indicating the test program is still being executed.

OPERATOR INPUTS

The program may be entered at either the Initial entry point (:200 - :20F) or the Restart entry point (:210 - :21F). (Either entry point may be accessed through any of the 16 locations mentioned, thus avoiding the necessity of resetting the Alpha 16 data switches to enter the address into the P register.) In both cases, the following queries are output to the teletype, and require a response through the keyboard. Default responses may be entered by typing a single carriage return or "#" character.

If the program is entered at the Initial entry point (: 200), a default response will indicate the standard default (described below within each query description). If the program is entered at the Restart entry point (: 210), a default response will indicate the previous response given to the query.

An entry is normally terminated with a carriage return and multiple responses to a query (e.g., Tests) must be separated by commas.

An erroneous input may be corrected by input of a back arrow (←) character, followed by the corrected input.

An input of an up arrow (↑) character will cause the previous (current -1) query to be reprinted.

A "#" character may be used at any time in place of the carriage return. This will cause the program to skip all subsequent queries and assume default responses for each of them.

[illegible]

MESSAGE	INPUT
TSTS=	Up to 14 letters, separated by commas, and terminated with a carriage return or "#" character, representing the tests to be run, in the order of input. A letter may be repeated, which will cause the test to be repeated. The standard default is all tests (A-N) to be run consecutively.
CYLS= 203 406	Number of cylinders in decimal, terminated with a carriage return or "#" character. Allowable inputs range from 1 to 408. Standard default is 203 cylinders. NOTE If the user wishes to test only a particular cylinder or group of consecutive cylinders, he may enter the starting and ending cylinder numbers, in decimal, as additional parameters. For example, a response of "203,0,9CR" will cause only cylinders 0 through 9 to be tested. An input of "203,4CR" will cause only cylinder 4 to be tested.
RAND=	Two hexadecimal values to be used in Test F to initialize the random number generators to a known value; separated by a comma, and terminated with a carriage return or "#" character. Note that the two inputs may not be "0,0" or "0,1".

MESSAGE | INPUT

Standard default is "1234,0002 CR". A default response after entry through the Restart entry point (:210) signifies that the random number generator is not to be re-initialized.

NOTE

If Test F is run more than once, new starting random numbers (generated from the previous numbers) will be used for each pass through the test. If the user wishes to re-initialize the random numbers for each pass, a third parameter (the letter "R") must be input. For example, "9ABC, DEF0, R CR" will cause the random numbers to be re-initialized to their starting values upon each entry into Test F.

4,

HDS= 4#

(4,2,3) upper

Number of heads, in decimal, terminated with a carriage return or "#" character. Allowable input is 1-20. Standard default is 2 heads.

NOTE

If the user wishes to test only a particular head or group of consecutive heads, he may enter the starting and ending head numbers, in decimal, as additional parameters. For example, a response of "4,2,3CR" will cause only the last two heads (the second platter) to be tested. An input of "4,0" will cause only head 0 to be tested.

PROC =

Processor type and memory speed, in decimal, terminated with a carriage return or "#" character, according to the following table:

	Speed				
Type	Unknown	C1600	C1200	C980	SC1200
Alpha 16	--	0	--	--	--
LSI-1	1	3	5	7	9
LSI-2	2	4	6	8	10

MESSAGE	INPUT
	If the "unknown" code is entered, tests K through N, and Section 1 of Test I will not be executed as these tests are dependent on memory speed. Standard defualt is "4" (LSI-2, C1600 memory).
INTS?	"Y" or "N" (yes or no) terminated with a carriage return or "#" character, to perform each test under interrupt control. (Note that Tests K through N will not use interrupts in any case. Also, if interrupts are requested, the Real Time Clock, if present, will be enabled for word interrupts during the running of the program.) Standard default is "Y" (test with interrupts).
PATN=	One to four hexadecimal digits, representing a one-word data pattern to be used in Tests C and E, terminated with a carriage return or "#" character. Standard default is :0000.
UNITS=	One to four decimal unit numbers (in the range 0-3) separated by commas and terminated with a carriage return or "#" character. The order of unit testing is determined by the order of input, and unit numbers may be repeated. Standard default is unit 0 only.
SECS=	Number of sectors per track in decimal, terminated with a carriage return or "#" character. Allowable input is 1 - 24. Standard default is 12 sectors per track.
WDS=	Number of words per sector in decimal terminated with a carriage return or "#" character. Allowable input is 12 - 256. Standard default is 256 words per sector.
INT LC=	Disk interrupt location in hexadecimal, terminated with a carriage return or "#" character. Allowable input is any address in the range :2 - :8E or :100 - :1FE. Standard default is location A (hexadecimal).
DEV AD=	Disk device address in hexadecimal terminated with a carriage return or "#" character. Standard default is device address F (hexadecimal).

[illegible]

OPTIONS

The operator may, at any time, set or reset any combination of SENSE Switch and Console data bits 0 through 3, to enable or disable the following options:

DATA BIT	OPTION
0	If performing a write data or read data function, include a dump of the data buffer at the end of each error report. This bit is tested upon occurrence of each error. The buffer dump may be aborted by resetting this bit after the dump has begun.
1	Suppress all error messages. This will override bit 0 if both 0 and 1 are set. This bit is tested upon occurrence of each error.
2	Dump data miscompare and CRC error tallies for each on-line unit, in decimal, upon completion of each test. The dump will include: 1. Pass number 2. Unit number 3. Number of accumulated "hard" errors (CRC error occurred 3 or more times out of 5 tries or data miscompare occurred twice out of two tries). 4. Number of accummulated "soft" errors (CRC error occurred no more than twice out of five tries, or data miscompare occurred once out of two tries). 5. Number of accumulated bit miscompares (hard data miscompare errors only). This bit is tested at the end of each test.
3	Run test continuously. This bit is tested upon completion of the last requested test for the last requested unit. (This option does not reset the error tallies.)

NOTE

If bit 3 is not set at end-of-pass, an end-of-test message ("EOT") will be output, followed by a halt. If RUN is subsequently depressed, the program will continue at the Restart entry point (:210).

DATA BIT	OPTION
Sense Switch (set)	Suppress output of test titles, unit number, and pass number. This does not affect output of error messages.

NOTE

Entering the program at the Initial entry point (:200) resets the pass counter and the error tallies; entering at the Restart entry point (:210) leaves these counters unchanged.

ERROR HANDLING

When a disk error condition occurs, a standardized error report is output to the teletype (unless suppressed by data bit 1 set) after which the test continues. In addition to the error report, certain status errors require special operations (restore, retry function, etc.) which are noted below.

Error Report Contents

1. Error number (refer to Error List for interpretation).
2. A 16-bit binary representation of the disk status word (if status error) where each "1" bit, read from right to left, corresponds to the following status:

Bit Set	Status	
0	Controller Busy	
1	No ID Compare	
2	ID CRC Error	
3	Data CRC Error	
4	End of Cylinder	
5	Illegal Head Address	
6	DMA Rate Error	
7	Time out period exceeded	
8	Drive not ready	
9	Drive unsafe (write check)	
10	Seek Error	
11	Incomplete Seek, unit 0	meaningful only for the unit currently being tested
12	Incomplete Seek, unit 1	
13	Incomplete Seek, unit 2	
14	Incomplete Seek, unit 3	
15	Write Protect Error	

3. Current Test
4. Pass Number
5. Unit Number
6. Function being tested. Note that if function is "Restore", no further information is output.
7. Cylinder, Head, and Sector in hexadecimal.
8. I/O length in hexadecimal.
9. Buffer address in memory in hexadecimal.
10. I/O data length, in hexadecimal.
11. Number of words not transferred, in hexadecimal.

In addition to the above data, which is output in each report, further information may be included depending on the particular test and/or type of failure. This additional data is described within each description in the error list.

ERROR RECOVERY

Initiation of each I/O operation is followed by a delay of approximately one second (or approximately 5 seconds for a Restore function),to permit completion of the operation Once the I/O operation has terminated (or the delay expires, in which case error 00001 or 00002 is output), the I/O status word is input and different logic paths are then taken depending on the status, as follows: (Refer to Error Report Contents for the meaning of each error bit.)

1. Bit 2 is checked first, then bit 3 (ID and Data CRC errors). If either is on, error 00005 or 00006 is output, followed by the message "RETRY". Then the I/O operation is repeated four times and an additional error 00005 or 00006 is output on each additional instance of a CRC error. After the four retries, an "END RETRY" message is output, a Restore function is issued, the error tallies are updated, and the current test continues.

2. After it has been established that no CRC error condition exists, each bit in the status word is checked, beginning with bit 0 (controller busy), and ending with bit 15 (Write Protect error). Note that bits 11-14 (Incomplete Seek) are masked off, except for the bit pertaining to the current unit. When a bit is found on, the error report (0003-00018) is output, a Restore function is issued and the current test continues.

3. During the Read portion of tests C,E,F,G and H, the input data is compared to the expected data for that test, and a miscompare will cause output of error 00019 and/or 00020, after which the message "REREAD" is output and the Read operation is repeated once. (A second error 00019 or 00020 is output if the miscompare recurs.) After the repeated Read operation, the message "END REREAD" is output, the error tallies are updated and

the current test continues. Note that since status is also checked in a "Reread" sequence, it is possible for a CRC error to cause a "Retry" within a "Reread"; i.e.,

"REREAD"
"RETRY"
"END RETRY"
"END REREAD"

Note that in test E,F and G, a ten-word data field, consisting of five 2-word ID images, is included as the first ten words of the data. A data miscompare within this ten-word field causes Error 00019 to be output.

4. Specialized types of errors (00021 - 00040), each of which occurs only in one particular test, do not cause the I/O operation to be retried.

ERROR LIST

ERROR NUMBER	DESCRIPTION
ER 00000	A Controller Not Busy status was not sensed after occurrence of an I/O interrupt. Additional error report data: None
ER 00001	A Controller Not Busy status (or Seek Complete Status if a Seek function) was not sensed within approximately one second (or approximately 5 seconds if a Restore function) after initiation of an I/O operation. Additional error report data: None
ER 00002	An I/O interrupt did not occur within approximately one second after initiation of an I/O operation. Additional error report data: None
ER 00003	A Controller Busy status was input following an I/O operation Additional error report data: 1. 3-word ID read from disk 2. Buffer dump, unless function was Restore or Write Format
ER 00004	A No ID Compare status was input following an I/O operation.

ERROR NUMBER	DESCRIPTION
	Additional error report data: 1. 3-word ID read from disk 2. Buffer dump, unless function was Restore or Write Format
ER 00005	An ID CRC Error Status was input following an I/O operation. (The function will be retried four times.)
	Additional error report data: 1. 3-word ID read from disk 2. Buffer dump, unless function was Restore or Write Format
ER 00006	A Data CRC Error status was input following an I/O operation. (The function will be retried four times.)
	Additional error report data: 1. 3-word ID read from disk 2. Buffer dump, unless function was Restore or Write Format
ER 00007	An End-of-Cylinder Error status was input following an I/O operation.
	Additional error report data: 1. 3-word ID read from disk 2. Buffer dump, unless function was Restore or Write Format
ER 00008	A Head Address Error status was input following an I/O operation.
	Additional error report data: 1. 3-word ID read from disk 2. Buffer dump, unless function was Restore or Write Format
ER 00009	A Rate Error status was input following an I/O operation.
	Additional error report data: 1. 3-word ID read from disk 2. Buffer dump, unless function was Restore or Write Format

ERROR NUMBER	DESCRIPTION
ER 00010	A Time-Out Error status was input following an I/O operation. Additional error report data: 1. 3-word ID read from disk 2. Buffer dump, unless function was Restore or Write Format
ER 00011	A Drive Not Ready Error status was input following an I/O operation. Additional error report data: 1. 3-word ID read from disk 2. Buffer dump, unless function was Restore or Write Format
ER 00012	A Drive Unsafe Error status was input following an I/O operation. Additional error report data: 1. 3-word ID read from disk 2. Buffer dump, unless function was Restore or Write Format
ER 00013	A Seek Error status was input following an I/O operation. Additional error report data: 1. 3-word ID read from disk 2. Buffer dump, unless function was Restore or Write Format
ER 00014	An Incomplete Seek (Unit 0) Error status was input following an I/O operation. Additional error report data: 1. 3-word ID read from disk 2. Buffer dump, unless function was Restore or Write Format
ER 00015	An Incomplete Seek (Unit 1) Error status was input following an I/O operation. Additional error report data: 1. 3-word ID read from disk 2. Buffer dump, unless function was Restore or Write Format

ERROR NUMBER	DESCRIPTION
ER 00016	An Incomplete Seek (Unit 2) Error status was input following an I/O operation. Additional error report data: 1. 3-word ID read from disk 2. Buffer dump, unless function was Restore or Write Format
ER 00017	An Incomplete Seek (Unit 3) Error status was input following an I/O operation. Additional error report data: 1. 3-word ID read from disk 2. Buffer dump, unless function was Restore or Write Format
ER 00018	A Write Protect Error status was input following an I/O operation. Additional error report data: 1. 3-word ID read from disk 2. Buffer dump, unless function was Restore or Write Format
ER 00019	The first ten words input during a read operation, consisting of five 2-word ID images: Word 1 = Cylinder Word 2 = Sector/Head did not compare to the disk address read from. Additional error report data: 1. 3-word ID read from disk 2. First ten words of the input (ID images). 3. If Test F, the two initial random numbers used to generate the I/O data. 4. Buffer dump 5. If test F, Expected Buffer Dump
ER 00020	A data miscompare occurred during a read operation, within the test data following the ten word ID written to the disk.

ERROR NUMBER	DESCRIPTION
	Additional error report data: 1. Address of the first input data word in error. 2. The first input data word in error. 3. The expected data word. 4. If Test F, the two initial random numbers used to generate the I/O data. 5. Buffer dump. 6. If test F, Expected Buffer Dump
ER 00021	Test A error. The cylinder number input during a Read ID operation miscompared to the number of the cylinder read from. Additional error report data: 1. 3-word ID read from disk
ER 00022	Test B error. An ID read from the disk during the first Read ID operation miscompared to the expected ID. Additional error report data: 1. Buffer dump (buffer contains the ID input from the Read ID operation).
ER 00023	Test B Error. An End of Cylinder status was not input upon termination of the second Read ID operation. Additional error report data: 1. Buffer dump (buffer contains the ID input from the Read ID operation).
ER 00024	Test B error. An ID read from the disk during the second Read ID operation miscompared to the expected ID. Additional error report data: 1. Buffer dump (buffer contains the ID input from the Read ID operation).
ER 00025	Test D error. The I/O times for a Seek and a 2-word Read ID operation on an Alpha 16 or LSI-2 system were not within 87.5% - 112.5% of each other.

ERROR NUMBER	DESCRIPTION
	Additional error report data: 1. Seek time. 2. Read ID time. 3. Read data time. 4. Buffer dump.
ER 00026	Test D error. The I/O time for a 2-word Read Data operation was less than 87.5% of the Seek time to the same disk address. Additional error report data: 1. Seek time. 2. Read ID time. 3. Read Data time. 4. Buffer dump.
ER 00027	Test D error. The I/O time for a 2-word Read ID operation on an LSI-1 system was greater than 12.5% of the Seek time to the same disk address. Additional error report data: 1. Seek time. 2. Read ID time. 3. Read Data time. 4. Buffer dump
ER 00028	Test D error. The I/O time counter overflowed (incremented past 65,535) during an I/O operation (Seek, Read ID, or Read Data), causing the counter to return to a value of a zero. Additional error report data: 1. Seek time. 2. Read ID time. 3. Read Data time. 4. Buffer dump.
ER 00029	Test H error. The actual data CRC word input following the Write operation was not equal to :0001 as expected. Additional error report data: 1. CRC word input. 2. Buffer dump.
ER 00030	Test I, Section 1 error. A Seek operation to cylinder 0 was not completed within approximately 100 microseconds. Additional error report data: None

ERROR NUMBER	DESCRIPTION
ER 00031	Test I, Section 1 error. A Seek operation to cylinder 200 was completed in less than approximately 30 milliseconds. Additional error report data: None
ER 00032	Test I, Section 1 error. A Seek operation to cylinder 200 was not completed within approximately 300 milliseconds. Additional error report data: None
ER 00033	Test I, Section 2 error. The cylinder number input in a Read ID operation miscompared to the cylinder number addressed. Additional error report data: 1. 3-word ID read from disk 2. Cylinder number in counter A 3. Cylinder number in counter B
ER 00034	Test J error. A No ID Compare status was not input after issuance of a Read function to a non-existent sector. Additional error report data: None
ER 00035	Test J error. An Illegal Head Address/No ID Compare status was not input after issuance of a Read function to a non-existent cylinder. Additional error report data: None
ER 00036	Test J error. A Seek Error status was not input after issuance of a Read function to a non-existent cylinder. Additional error report data: None
ER 00037	Test K error. Incorrect timing occurred. See test description for timing limits.

ERROR NUMBER	DESCRIPTION
	Additional error report data: 1. Time for second Read operation. 2. Expected timing range. 3. Revolution time. 4. Single sector time. 5. Buffer dump. Note that all times are in 100 microsecond increments.
ER 00038	Test L error. Incorrect timing occurred. See test descriptio for timing limits. Additional error report data: 1. Time for second Read operation. 2. Expected timing limit. 3. Revolution time. 4. Single sector time. 5. Buffer dump. Note that all times are 100 microsecond increments.
ER 00039	Test M error. Incorrect timing occurred. See test description for timing limits. Additional error report data: 1. Time for second Read operation 2. Expected timing limit. 3. Revolution time. 4. Single Sector time. 5. Buffer dump. Note that all times are in 100 microsecond increments.
ER 00040	Test N error. Incorrect timing occurred. See test description for timing limits. Additional error report data: 1. Time for second Read operation 2. Expected timing limit. 3. Revolution time. 4. Single sector time. 5. Buffer dump.

Note that all times are in 100 microsecond increments.

BUFFER PRESETS

Prior to issuing a read function to the disk, it is desirable to preset the input buffer to something other than the expected input data, so that the data transfer is apparent. Therefore, in tests E, F, G and H, the preset data will be the complement of the requested user pattern. The buffer is not preset in the other tests.

WORST CASE PATTERNS

The following can be considered worst case patterns for the Disk. Use of a particular pattern will depend on the disk logic one wishes to test most thoroughly:

0	Produces highest amplitude, lowest frequency.
:FFFF	Produces lowest amplitude, highest frequency.
:333	Worst case for peak shift.
:39CE	Worst case for one-bit amplitude.

I/O CONTROL BLOCK (IOB)

I/O operations are initiated by means of an OTA or OTX instruction to the disk, where the A or X register contains the address of a four-word I/O Control Block (IOB), containing the following information:

Word 1:

Bits 15-8	Sector number
Bits 7-0	Head number.

Word 2:

Bits 15-8	Cylinder number	
Bit 7	High order bit of the cylinder number (0 if the cylinder number is less than 256; 1 if the cylinder number is 256 or greater).	
Bits 6-5	Zero	
Bits 4-2	Function Code:	
	000	No-op
	001	Read Data
	010	Read Identifier
	011	Verify
	100	Write Data
	101	Write Format
	110	Seek only
	111	Read data, hog mode
Bits 1-0	Unit number (0-3)	

Word 3: I/O Word length

Word 4: I/O Data Buffer address.

Note that the Restore function is initiated by a Select command, using a function code of 4.

MOVING HEAD DISK FORMATTER

REFERENS

INTRODUCTION

This document describes the Formatter Package for the moving head disk. The package consists of a supervisor program, which accepts parameters from the user via the teletype keyboard, and the formatting routine itself. The package requires a moving head disk unit and controller utilizing device address :F.

USAGE

The supervisor program and the formatting routine each reside on paper tape in ALPHA-16 object code format. The two programs may be loaded and linked by the LAMBDA object loader, or the formatting routine may be used alone as an external subroutine to a user's program.

DESCRIPTION

Supervisor Program

The supervisor program is entered at relative location 0, and outputs several queries via the teletype, as follows:

Query	Operator Input (Decimal)
Sects=	Input sectors per track (10 or 12) and terminate with a period. Period only signifies 12 sectors.
Heads=	Input number of heads (tracks per cylinder: 2, 4 or 20) and terminate with a period. Period only signifies 2 heads.
Cylrs=	Input number of cylinders per unit (200 or 400) and terminate with a period. Period only signifies 200 cylinders.
Unit=	Input unit to be formatted (0-3) and terminate with a period. Period only signifies unit 0.
Full Fmat?	Input "Y" to format the entire disk unit. Input "N" to format only certain cylinders. If "Y", the remaining queries are by-passed.

1st Cyl=	Input number of first cylinder to be formatted, terminated by a period. Period only signifies cylinder 0. Note that this input must be less than total number of cylinders.
Last Cyl=	Input number of last cylinder to be formatted, terminated by a period. Period only signifies cylinder 0. Note that this input must be less than total number of cylinders, but not less than first cylinder to be formatted.
Flag Bits=	The "User Flag Bits" is a two-bit field included in the cylinder headers, which may be set to 0, 1, 2 or 3. Any subsequent accessing of the cylinders to be formatted (as when using the disk drivers) requires that these bits be set to the same settings as when formatted. Input 0-3, terminated with a period. Period only signifies a setting of zero.
Write Prot?	The write protect bit is similar to the User Flag Bits above, in that when accessing a protected cylinder via the disk driver, the bit must be set when writing data, but not when reading or verifying. Input "Y" to write-protect the cylinders being formatted. Otherwise input "N".

When the above queries are satisfied, the supervisor program branches to the formatting routine (see "Formatting Routine" below). When the supervisor program regains control, one or more of the following messages will be printed on the teletype and the program will halt. Depress RUN to restart the supervisor program.

1. "ALT CYLS USED" - This is not an error message, but only an indication that one or more alternate cylinders were used.

2. "CYL 0 BAD" - an alternate cylinder was formatted for cylinder 0; this means the Autoload feature cannot be used on this disk cartridge, since cylinder 0 is defective.

3. "FORMAT COMPLETE" - The formatter program has completed its operation without error, although alternate cylinders may have been required.

4. "BAD PARAMETER" - an illegal response was input by the operator to one of the queries output in the calling program.

5. "ALTS EXHAUSTED" - CRC errors were encountered when trying to format a cylinder causing the format routine to attempt to use an alternate cylinder. This message indicates that there were insufficient alternates available.

6. If a hardware error is encountered, one or more error messages will be printed. The possible messages are:

```
NO ID COMPARE
END OF CYL
ILLEGAL ADDRESS
SEEK ERROR
RATE ERROR
WRITE PROTECTED
DRIVE NOT READY
DRIVE UNSAFE
```

FORMATTING ROUTINE

The formatting routine is coded as an external subroutine which may be linked to the supervisor program described above, or directly to the user's program. If the supervisor is not used, the formatting routine may be called directly by the user as follows:

GENERAL CALLING SEQUENCES

To branch from main memory:

```
DFMAT     REF
          LDA       LIST
          JST       *DFMAT
          Error Return
          Normal Return
```

To branch through scratchpad area:

```
          EXTR      DFMAT
          LDA       LIST
          JST       DFMAT
          Error Return
          Normal Return
```

(Previous contents of A and X registers will be lost)

Where LIST contains the address of a 3 or 6 word parameter list as follows:

Word 1:	Bits 0-4	Tracks per cylinder (Heads) (2,4 or 20)
	Bits 5-7	Zero
	Bits 8-11	Sectors per track (10 or 12)
	Bits 12-15	Zero

Word 2:		Number of cylinders (200 or 400)
Word 3:		
	Bit 0	0 to format entire disk cartridge 1 to format selected cylinders only
	Bits 1-7	Zero
	Bits 8-9	Unit number (0-3)
	Bits 10-15	Zero
Word 4: *		Starting cylinder number (must be less than word 2)
Word 5: *		Ending cylinder number (must be less than word 2 and not less than word 4)
Word 6: *		
	Bit 0	0 if not to be write-protected 1 if to be write-protected
	Bits 1-2	User's code (0-3). Must subsequently be used whenever accessing these cylinders.
	Bits 3-15	Zero

*Note: Words 4-6 are not necessary if formatting entire disk cartridge.

PROGRAM LOGIC

The format routine first examines each entry in the parameter list for legality, then proceeds to format and verify each cylinder specified. If a CRC error occurs during an I/O operation, the cylinder will be flagged as bad, and an alternate cylinder formatted.

For any error status which occurs, the I/O operation will be retried twice before returning with an error to the calling program.

STATUS CONDITIONS

When the error return is taken, the operation status will be contained in the A register as follows:

Bit Set	Description
0	Controller continuously busy
1	No ID compare
2	Illegal Parameter
3	Alternate cylinders exhausted

Bit Set	Description
4	End of Cylinder Error
5	Illegal address
6	Rate error
7	Write Protected
8	Drive not ready
9	Drive unsafe
10	Seek Error
11-15	Not used

If the normal return is taken, the A register will contain zero.

X register contents upon normal or error return:

X=0:	No alternate cylinders were used
X=1	One or more alternate cylinders were used, but cylinder zero (required for Autoload) did not need an alternate.
X=2	One or more alternate cylinders were used, and one of them was required for cylinder zero. (This means that the Autoload option cannot be used with this disk cartridge).

MOVING HEAD DISK DRIVER

INTRODUCTION

This document describes the general purpose DMA driver subroutine for the moving head disk. The program requires a formatted disk unit and controller utilizing device address :F.

USAGE

The program resides on paper tape in ALPHA-16 object code format. The program is coded as an external subroutine to be loaded and linked to a calling program, at load time, by the LAMBDA object loader.

GENERAL CALLING SEQUENCES

To branch from main memory:

```
MDISK       REF
            LDA         LIST
            JST         *MDISK
            Error Return
            Normal Return
```

To branch through scratchpad area:

```
            EXTR        MDISK
            LDA         LIST
            JST         MDISK
            Error Return
            Normal Return
```

(Previous contents of A and X registers will be lost.)

Where LIST contains the address of a 5 word parameter list in the user's program as follows:

PARAMETER LIST

Word 1:

Bits 0-5	Head number (0-19)*
Bits 6-7	Zero
Bits 8-11	Sector number (0-11)
Bits 12-15	Zero

Word 2

Bits 0-8	Cylinder number (0-399)
Bits 9-11	Zero
Bits 12-13	User flag bits (must match the flag bits used when formatting the cylinder)
Bits 14-15	Zero

Word 3:

Bits 0-1	Function:	0=Read 1=Write 2=Verify CRC 3=Write and Verify CRC
Bits 2-7	Zero	
Bits 8-9	Unit number (0-3)	
Bits 10-15	Zero	

Word 4:	Word length (1-32,767)
Word 5:	Address of I/O buffer in user's program

* NOTE

If it is necessary to write to a cylinder which has been formatted as "write-protected", add hexadecimal 20 to the head number.

A-REGISTER CONTENTS UPON RETURN

When an I/O operation is completed, the driver will return to the user with the status of the operation in the A register as follows:

If the error return is taken:

Bit Set	Description
0	Controller continuously busy
1	No ID compare
2	ID CRC error
3	Data CRC error
4	End of cylinder error
5	Illegal head address
6	Rate error
7	Write protected
8	Drive not ready
9	Drive unsafe
10	Seek error
11	Illegal parameter
12-15	Not used

If the normal return is taken the A register will contain zero.

X-REGISTER CONTENTS UPON RETURN

If the error return is taken, the X-register will contain the number of words not transferred, if a read or write operation was partially completed. Otherwise the X-register will be zero.

If the normal return is taken, the X-register will contain zero if no alternate cylinders were used, or non-zero if alternates were required.

If an error condition is sensed, the driver will retry the function twice (three tries in all) before returning an error status.

```
*MOVING HEAD DISK DRIVER         96082-10A0
*COPYRIGHT 1972 COMPUTER AUTOMATION INC
*
*          12/27/72
*THIS ROUTINE MAY BE CALLED AS FOLLOWS:
*MDISK  REF
*       LDA  LIST
*       JST  *MDISK
*      ERROR RETURN
*      NORMAL RETURN
*
*OR
*
*        EXTR MDISK
*        LDA  LIST
*        JST  MDISK
*      ERROR RETURN
*      NORMAL RETURN
*
*WHERE "LIST" IS THE ADDRESS OF A 5-WORD
*PARAMETER LIST AS FOLLOWS:
*
*WORD 1:
* BITS 15-8:     SECTOR (0-12)
* BITS 7-0:      HEAD (0-19)
*                NOTE: IF IT IS NECESSARY TO
*                WRITE TO A CYLINDER WHICH HAS
*                BEEN FORMATTED AS "WRITE-
*                PROTECTED", ADD HEX :20 TO
*                THE HEAD NUMBER.
*WORD 2:
* BITS 13-12:    USER FLAG BITS
* BITS 8-0:      CYLINDER (0-399)
*WORD 3:
* BITS 15-8:     UNIT (0-3)
* BITS 7-0:      FUNCTION:
*                0=READ
*                1=WRITE
*                2=VERIFY CRC
*                3=WRITE & VERIFY CRC
*WORD 4:         DATA LENGTH (1-32,767)
*WORD 5:         USER BUFFER ADDRESS
*
*IF A STATUS ERROR OCCURS DURING I/O, THE
*DRIVER WILL RETRY THE FUNCTION TWICE (THREE
*TRIES IN ALL) BEFORE RETURNING AN ERROR
*STATUS.  WHEN THE ERROR RETURN IS TAKEN, THE
*A-REGISTER WILL CONTAIN ONE OR MORE OF THE
*FOLLOWING BITS ON:
*BIT  0=CONTROLLER CONTINUOUSLY BUSY
*BIT  1=NO ID COMPARE
*BIT  2=ID CRC ERROR
*BIT  3=DATA CRC ERROR
*BIT  4=END OF CYLINDER ERROR
```

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*BIT  5=ILLEGAL ADDRESS
*BIT  6=RATE ERROR
*BIT  7=WRITE PROTECTED
*BIT  8=DRIVE NOT READY
*BIT  9=DRIVE UNSAFE
*BIT 10=SEEK ERROR
*BIT 11=ILLEGAL PARAMETER
*BIT 12-15= UNUSED
*
*IF THE NORMAL RETURN IS TAKEN, THE A-REGISTER
*CONTENTS WILL BE ZERO.
*
*THE X-REGISTER, FOR A NORMAL
*RETURN, WILL CONTAIN ZERO IF NO ALTERNATE
*CYLINDER WAS USED, OR 1 IF AN ALTERNATE
*CYLINDER WAS USED.
*
*FOR AN ERROR RETURN, THE X-REGISTER WILL
*CONTAIN THE NUMBER OF WORDS NOT TRANSFERRED,
*IF A READ OR WRITE OPERATION WAS PARTIALLY
*COMPLETED. OTHERWISE THE X-REGISTER WILL
*BE ZERO.
```

```
PAGE  0003
0078                        NAM  MDISK
0079  000C                  REL  0
0080        0000  MDISK     EQU  $
0081        000C  SECTS     EQU  12
0082        0014  HEADS     EQU  20
0083        00C8  CYLS      EQU  200
0084        000F  DA        EQU  :F         DEVICE ADDRESS
0085  0000  0800            ENT
0086  0001  0108            ZXR             CLEAR ALT CYL FLAG
0087  0002  EAD5            STX  ALTUSE
0088  0003  EAD5            STX  VERFLG     AND WRITE & VER FLAG
0089  0004  0048            TAX
0090  0005  B400            LDA  =0         GET SECTORS
0091  0006  9AC9            STA  IOB1
0092  0007  9ACC            STA  SAVB1
0093  0008  1307            LRA  8
0094  0009  92C2            SUB  SECTSP     LEGAL INPUT
0095  000A  2083            JAM  MD1        YES
0096  000B  B2DA  PRMRTN    LDA  H800       ILLEGAL PARAM
0097  000C  0108  BADRTN    ZXR
0098  000D  F70D            RTN  MDISK      RETURN ERROR
0099  000E  C6DF  MD1       LAP  :DF        GET HEADS
0100  000F  8400            AND  =0
0101  0010  92BC            SUB  HEADSP     LEGAL INPUT
0102  0011  30C6            JAP  PRMRTN     NO
0103  0012  B2D2            LDA  H1FF
0104  0013  8401            AND  =1         GET CYLS
0105  0014  9ABC            STA  IOB2
0106  0015  92B8            SUB  CYLSP      LEGAL CYLS
0107  0016  30CB            JAP  PRMRTN     NO
0108  0017  B2B9            LDA  IOB2       YES SET HIGH ORDER BIT
0109  0018  1357            LLA  8          IF ON
0110  0019  3201            JOR  $+2
0111  001A  A2C7            IOR  H80
0112  001B  9AB5            STA  IOB2
0113  001C  B401            LDA  =1         GET USER FLAG BITS
0114  001D  13D6            LRA  7
0115  001E  82C2            AND  H60
0116  001F  A2B1            IOR  IOB2
0117  0020  9AB0            STA  IOB2       STORE THEM
0118  0021  B402            LDA  =2         GET UNIT NO.
0119  0022  13D7            LRA  8
0120  0023  82B9            AND  H3
0121  0024  9AB7            STA  COUNT      SAVE IT
0122  0025  C704            LAM  4          SET UP SENSE FOR
0123  0026  82A1            AND  RESET1     SEEK COMPLETE COMMAND
0124  0027  A2B4            IOR  COUNT
0125  0028  9A9F            STA  RESET1
0126  0029  C603            LAP  3          GET FUNCTION CODE
0127  002A  8402            AND  =2
0128  002B  3102            JAN  $+3        FC=0
0129  002C  C604            LAP  4          YES SET READ FC
0130  002D  F209            JMP  MD2
0131  002E  00D0            DAR             FC=1
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0132 002F 3102           JAN  $+3
0133 0030 C610 MD9       LAP  :10      YES SET WRITE FC
0134 0031 F205           JMP  MD2
0135 0032 00D0           DAR           FC=2
0136 0033 3082           JAP  $+3      YES
0137 0034 DAA4           IMS  VERFLG   MUST BE THREE
0138 0035 F605           JMP  MD9      SET WRITE FC
0139 0036 C60C           LAP  :C       SET VERIFY FC
0140 0037 A299 MD2       IOR  IOB2     ADD FUNCTION TO IOB2
0141 0038 A2A3           IOR  COUNT    ALSO ADD UNIT
0142 0039 9A97           STA  IOB2
0143 003A 9A9A           STA  SAVB2
0144 003B B403           LDA  @3       GET DATA LENGFTH
0145 003C 20F1           JAM  PRMRTN   LEGAL LENGTH
0146 003D 9A94           STA  IOB3
0147 003E 9A97           STA  SAVB3
0148 003F B404           LDA  @4       YES GET BUFFER ADRESS
0149 0040 9A92           STA  IOB4
0150 0041 9A95           STA  SAVB4
0151 0042 FA62 MD7       JST  IO       DO I/O
0152 0043 F254           JMP  OUT      GOOD I/O. RETURN
0153 0044 C602           LAP  2        BAD I/O. IS IT ID COMPARE
0154 0045 AA95           XOR  SAVSTT
0155 0046 2103           JAZ  MD3      YES
0156 0047 B293 MD5       LDA  SAVSTT
0157 0048 5A79 WNT       INX  DA,1     GET WORDS NOT XFERRED
0158 0049 F63C           JMP  BADRTN+1 AND RETURN WITH ERROR
0159 004A C71D MD3       LAM  :1D      CHANGE FC TO READ ID
0160 004B 8285           AND  IOB2
0161 004C A292           IOR  H8
0162 004D 9A83           STA  IOB2
0163 004E B29C           LDA  BUFAD
0164 004F 9A83           STA  IOB4
0165 0050 C602           LAP  2        USE LENGTH OF 2 WDS
0166 0051 9A80           STA  IOB3
0167 0052 FA52           JST  IO       DO READ ID
0168 0053 0000           NOP
0169 0054 B27C           LDA  IOB2     SEE IF CYLS MATCH
0170 0055 AA96           XOR  BUF
0171 0056 13D6           LRA  7
0172 0057 310A           JAN  MD6
0173 0058 C680           LAP  :80      SEE IF BAD BIT ON
0174 0059 8293           AND  BUF+1
0175 005A 3117           JAN  MD4      YES DO ALTERNATE CYL STUFF
0176 005B C61C           LAP  :1C
0177 005C 8278           AND  SAVB2
0178 005D C010           CAI  :10      NO SEE IF WRITE FUNCTION
0179 005E F203           JMP  MD6      YES ERROR
0180 005F C620           LAP  :20      NO SEE IF WRITE PROT BIT ON
0181 0060 828C           AND  BUF+1
0182 0061 3102           JAN  $+3
0183 0062 C602 MD6       LAP  2        NO ITS AN ERROR
0184 0063 F61B           JMP  WNT
0185 0064 FA05           JST  MDA      SET UP IOB1
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PAGE  0005
0186  0065  B26F        LDA  SAVB2   RESTORE ORIGINAL IO BLOCK
0187  0066  9A6A        STA  IOB2
0188  0067  FA3D        JST  IO      GO DO I/O
0189  0068  F22F        JMP  OUT     GOOD I/O
0190  0069  F622        JMP  MD5     NO ERROR RETURN
0191  006A  0800  MDA   ENT          FIX IOB1 ROUTINE
0192  006B  A268        IOR  SAVB1   OLD IOB1 PLUS AR
0193  006C  9A63        STA  IOB1
0194  006D  B268        LDA  SAVB3
0195  006E  9A63        STA  IOB3
0196  006F  B267        LDA  SAVB4
0197  0070  9A62        STA  IOB4
0198  0071  F707        RTN  MDA     RETURN
0199  0072  C71D  MD4   LAM  :1D     DO ALT CYL STUFF
0200  0073  8278        AND  BUF
0201  0074  A269        IOR  H4      FIRST READ FROM BAD CYL
0202  0075  9A5B        STA  IOB2    TO GET ALT CYL ADRESS
0203  0076  B255        LDA  SECTSP  TRY ALL SECTORS
0204  0077  0310        NAR          UNTIL GOOD STATUS
0205  0078  9A71        STA  SECTCT
0206  0079  C6FF        LAP  255     START WITH SECTOR 0
0207  007A  8272        AND  BUF+1
0208  007B  9A54  MDB   STA  IOB1
0209  007C  FA28        JST  IO      GO DO I/O
0210  007D  F204        JMP  MDC     GOOD STATUS
0211  007E  B251  MDE   LDA  IOB1
0212  007F  8A64        ADD  H100    BUMP TO NEXT SECTOR
0213  0080  DA69        IMS  SECTCT  ALL SECTS TRIES
0214  0081  F606        JMP  MDB     NOT YET
0215  0082  B24B  MDC   LDA  CYLSP   SEE IF LEGAL ALT NO
0216  0083  9268        SUB  BUF
0217  0084  2082        JAM  $+3
0218  0085  9259        SUB  H8
0219  0086  2083        JAM  MD8
0220  0087  B262        LDA  SECTCT
0221  0088  2166        JAZ  MD6
0222  0089  F60B        JMP  MDE
0223  008A  B261  MD8   LDA  BUF     YES OK
0224  008B  DA4C        IMS  ALTUSE  OK BUMP ALT CYL FLAG
0225  008C  1357        LLA  8
0226  008D  3201        JOR  $+2     SET UP ALT CYL ADRESS
0227  008E  A253        IOR  H80
0228  008F  9A4C        STA  COUNT   SAVE IT TEMPORARILY
0229  0090  C67F        LAP  :7F
0230  0091  8243        AND  SAVB2   GET THE FC, UNIT, ETC
0231  0092  A249        IOR  COUNT
0232  0093  9A3D        STA  IOB2    SET UP NEW IOB2
0233  0094  9A40        STA  SAVB2
0234  0095  C640        LAP  :40     SET ALTERNATE BIT
0235  0096  FE2C        JST  MDA     GO SET UP IOB1
0236  0097  F655        JMP  MD7     GO DO I/O AGAIN
0237  0098  B240  OUT   LDA  VERFLG  WAS VERIFY WANTED TOO
0238  0099  2108        JAZ  OUT3    NO
0239  009A  0110        ZAR          YES
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PAGE  0006
0240  009B  9A3D          STA   VERFLG   CLEAR THE FLZG
0241  009C  C71D          LAM   :1D      SET VERIFY FC
0242  009D  8237          AND   SAVB2
0243  009E  A241          IOR   HC
0244  009F  9A31          STA   IOB2
0245  00A0  9A34          STA   SAVB2
0246  00A1  F65F          JMP   MD7      AND DO I/O
0247  00A2  E235  OUT3    LDX   ALTUSE   WAS ALT CYL USED
0248  00A3  DEA3  OUT1    IMS   MDISK    IF NO ERRORS
0249  00A4  F7A4          RTN   MDISK    RETURN
0250  00A5  0800  IO      ENT            I/O SUBROUTINE
0251  00A6  C703  IOA     LAM   3        3 TRIES
0252  00A7  9A34          STA   COUNT
0253  00A8  B226  IOC     LDA   IOBAD    GET ADRESS OF IO BLOCK
0254  00A9  6D78          WRA   DA,0     SELECT DISK
0255  00AA  0108          ZXR            RESET TIMEOUT PTR
0256  00AB  4878  IOG     SSN   DA,0     BUSY
0257  00AC  F202          JMP   IOD      NO
0258  00AD  0128          IXR            YES BUMP COUNT
0259  00AE  3843          JXN   IOG      CHECK AGAIN
0260  00AF  5878  IOD     INA   DA,0     GET STATUS
0261  00B0  8229          AND   STMASK   MASK EXTRANEOUS BITS
0262  00B1  9A29          STA   SAVSTT   SAVE INPUT
0263  00B2  3089          JAP   IOE      WRITE PROTECT ON
0264  00B3  8235          AND   H7FFF    YES MOVE BIT
0265  00B4  9A26          STA   SAVSTT
0266  00B5  B21F          LDA   SAVB2    IS THIS WRITE MODE
0267  00B6  8230          AND   H1C
0268  00B7  AA30          XOR   H10
0269  00B8  3103          JAN   IOE      NO FORGET ABOUT IT
0270  00B9  B221          LDA   SAVSTT   YES SET BIT 7 ON
0271  00BA  A227          IOR   H80
0272  00BB  9A1F          STA   SAVSTT
0273  00BC  B21E  IOE     LDA   SAVSTT   RESTORE STATUS
0274  00BD  2107          JAZ   IOF      ANY ERRORS
0275  00BE  1355          LLA   6        YES SEE IF SEEK ERROR
0276  00BF  3201          JOR   $+2      NO
0277  00C0  FA05          JST   RESET    YES RESTORE
0278  00C1  DA1A          IMS   COUNT    IS THIS 3RD TRY
0279  00C2  F61A          JMP   IOC      NOT YET
0280  00C3  B217          LDA   SAVSTT   YES GET STATUS BACK IN
0281  00C4  DE1F          IMS   IO       BUMP TO BAD RETURN
0282  00C5  F720  IOF     RTN   IO       RETURN
0283  00C6  0800  RESET   ENT            RESTORE DISK SUBROUTINE
0284  00C7  407C          SEL   DA,4     INITIALIZE DISK
0285  00C8  497C  RESET1  SEN   DA,4     SEEK COMPLETE
0286  00C9  F601          JMP   $-1      NO
0287  00CA  5878          INA   DA,0     GET STATUS
0288  00CB  F705          RTN   RESET    YES RETURN
0289  00CC  000C  SECTSP  DATA  SECTS
0290  00CD  0014  HEADSP  DATA  HEADS
0291  00CE  00C8  CYLSP   DATA  CYLS
0292  00CF  00D0  IOBAD   DATA  IOB1
0293  00D0  0000  IOB1    DATA  0
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PAGE  0007
0294  00D1  0000  IOB2    DATA 0
0295  00D2  0000  IOB3    DATA 0
0296  00D3  0000  IOB4    DATA 0
0297  00D4  0000  SAVB1   DATA 0
0298  00D5  0000  SAVB2   DATA 0
0299  00D6  0000  SAVB3   DATA 0
0300  00D7  0000  SAVB4   DATA 0
0301  00D8  0000  ALTUSE  DATA 0
0302  00D9  0000  VERFLG  DATA 0
0303  00DA  877F  STMASK  DATA :877F
0304  00DB  0000  SAVSTT  DATA 0
0305  00DC  0000  COUNT   DATA 0
0306  00DD  0003  H3      DATA 3
0307  00DE  0004  H4      DATA 4
0308  00DF  0008  H8      DATA 8
0309  00E0  000C  HC      DATA :C
0310  00E1  0060  H60     DATA :60
0311  00E2  0080  H80     DATA :80
0312  00E3  00C4  HC4     DATA :C4
0313  00E4  0100  H100    DATA :100
0314  00E5  01FF  H1FF    DATA :1FF
0315  00E6  0800  H800    DATA :800
0316  00E7  001C  H1C     DATA :1C
0317  00E8  0010  H10     DATA :10
0318  00E9  7FFF  H7FFF   DATA :7FFF
0319  00EA  0000  SECTCT  DATA 0
0320  00EB  00EC  BUFAD   DATA BUF
0321  00EC  0000  BUF     DATA 0,0
      00ED  0000
0322        0000          END  MDISK
0000  ERRORS
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PAGE  0008
   ALTUSE   00D8        BADRTN   000C        BUFAD    00EB        BUF      00EC
   COUNT    00DC        CYLSP    00CE        CYLS     00C8        DA       000F
   HC       00E0        HC4      00E3        HEADSP   00CD        HEADS    0014
   H1C      00E7        H1FF     00E5        H10      00E8        H100     00E4
   H3       00DD        H4       00DE        H60      00E1        H7FFF    00E9
   H8       00DF        H80      00E2        H800     00E6        IOA      00A6
   IOBAD    00CF        IOB1     00D0        IOB2     00D1        IOB3     00D2
   IOB4     00D3        IOC      00A8        IOD      00AF        IOE      00BC
   IOF      00C5        IOG      00AB        IO       00A5        MDA      006A
   MDB      007B        MDC      0082        MDE      007E      X MDISK    0000
   MD1      000E        MD2      0037        MD3      004A        MD4      0072
   MD5      0047        MD6      0062        MD7      0042        MD8      008A
   MD9      0030        OUT      0098        OUT1     00A3        OUT3     00A2
   PRMRTN   000B        RESET    00C6        RESET1   00C8        SAVB1    00D4
   SAVB2    00D5        SAVB3    00D6        SAVB4    00D7        SAVSTT   00DB
   SECTCT   00EA        SECTSP   00CC        SECTS    000C        STMASK   00DA
   VERFLG   00D9        WNT      0048
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PAGE  0001
     0301   ALTUSE     0087* 0224* 0247
     0097   BADRTN     0158
     0321   BUF        0170  0174  0181  0200  0207  0216  0223  0320
     0320   BUFAD      0163
     0305   COUNT      0121* 0124  0141  0228* 0231  0252* 0278*
     0083   CYLS       0291
     0291   CYLSP      0106  0215
     0084   DA         0157  0254  0256  0260  0284  0285  0287
     0317   H10        0268
     0313   H100       0212
     0316   H1C        0267
     0314   H1FF       0103
     0306   H3         0120
     0307   H4         0201
     0310   H60        0115
     0318   H7FFF      0264
     0308   H8         0161  0218
     0311   H80        0111  0227  0271
     0315   H800       0096
     0309   HC         0243
     0312   HC4
     0082   HEADS      0290
     0290   HEADSP     0101
     0250   IO         0151* 0167* 0188* 0209* 0281* 0282
     0251   IOA
     0293   IOB1       0091* 0193* 0208* 0211  0292
     0294   IOB2       0105* 0108  0112* 0116  0117* 0140  0142* 0160
                       0162* 0169  0187* 0202* 0232* 0244*
     0295   IOB3       0146* 0166* 0195*
     0296   IOB4       0149* 0164* 0197*
     0292   IOBAD      0253
     0253   IOC        0279
     0260   IOD        0257
     0273   IOE        0263  0269
     0282   IOF        0274
     0256   IOG        0259
     0099   MD1        0095
     0140   MD2        0130  0134
     0159   MD3        0155
     0199   MD4        0175
     0156   MD5        0190
     0183   MD6        0172  0179  0221
     0151   MD7        0236  0246
     0223   MD8        0219
     0133   MD9        0138
     0191   MDA        0185* 0198  0235*
     0208   MDB        0214
     0215   MDC        0210
     0211   MDE        0222
N    0080   MDISK      0078  0098  0248* 0249  0322
     0237   OUT        0152  0189
     0248   OUT1
     0247   OUT3       0238
     0096   PRMRTN     0102  0107  0145
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PAGE  0002
    0283  RESET     0277* 0288
    0285  RESET1    0123  0125*
    0297  SAVB1     0092* 0192
    0298  SAVB2     0143* 0177  0186  0230  0233* 0242  0245* 0266
    0299  SAVB3     0147* 0194
    0300  SAVB4     0150* 0196
    0304  SAVSTT    0154  0156  0262* 0265* 0270  0272* 0273  0280
    0319  SECTCT    0205* 0213* 0220
    0081  SECTS     0289
    0289  SECTSP    0094  0203
    0303  STMASK    0261
    0302  VERFLG    0088* 0137* 0237  0240*
    0157  WNT       0184
0322 SOURCE LINES
```